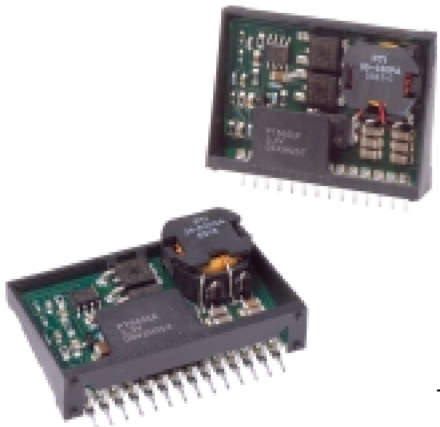
5-A 12 /24-V Input Adjustable Integrated Switching Regulator

SLTS038B -FEBRUARY 1999 - REVISED MARCH 2004



Features

- Single Device: 5-A Output
- Input Voltage Range: 9 V to 28 V
- 12 V / 24 V Input Compatible
- Adjustable Output Voltage
- 80 % Efficiency
- Output Remote Sense
- On/Off Standby Function

Description

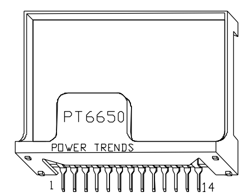
The PT6650 power modules are a series of high efficiency, non-isolated step-down integrated switching regulators (ISRs). These regulators are designed to operate over a 9 V to 28 V input voltage range to produce a tightly regulated output voltage at load currents of up to 5 A. The wide input voltage range allows them to operate off either a 12 V or 24 V DC input bus system, making them ideal for general purpose and industrial applications. The series includes standard output voltage options ranging from 15 V down to 2.5 V, and down to 1.8 V with adjustment. Only two external capacitors are required for proper operation.

The PT6650 series is housed in a low-cost 14-pin SIP (Single In-line Package) and is available in both vertical and horizontal configurations, including surface-mount.

Ordering Information

PT6651❒ = 3.3 Volts
PT6652❒ = 2.5 Volts
PT6653❒ = 5 Volts
PT6654❒ = 9 Volts
PT6655❒ = 15 Volts
PT6656❒ = 12 Volts

Note: Back surface of product is conducting metal



PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code *
Vertical	P	(EED)
Horizontal	D	(EEA)
SMD	E	(EEC)
Horizontal, 2-Pin Tab	M	(EEM)
SMD, 2-Pin Tab	L	(EEL)
Horizontal, 2-Pin Ext Tab	Q	(EEQ)
SMD, 2-Pin Ext Tab	F	(EEF)
Vertical, Side Tab	R	(EEE)
Horizontal, Side Tab	G	(EEG)
SMD, Side Tab	B	(EEK)

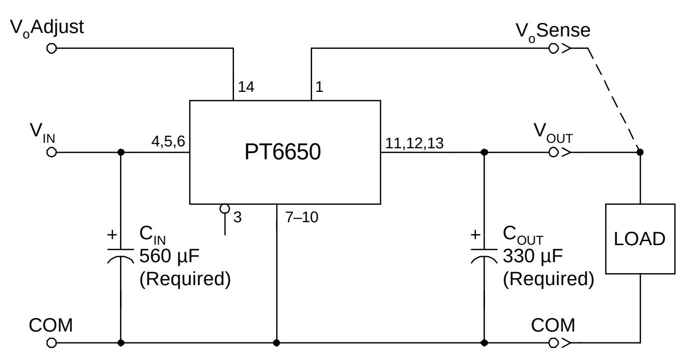
** Previously known as package styles 400/410.*
(Reference the applicable package code drawing for the dimensions and PC board layout)

Pin-Out Information

Pin	Function
1	Remote Sense
2	Do Not Connect
3	STBY*
4	Vin
5	Vin
6	Vin
7	GND
8	GND
9	GND
10	GND
11	Vout
12	Vout
13	Vout
14	V_O Adjust *

* *For further information, see application notes.*

Standard Application



C_{in} = Required 560 µF electrolytic
C_{out} = Required 330 µF electrolytic

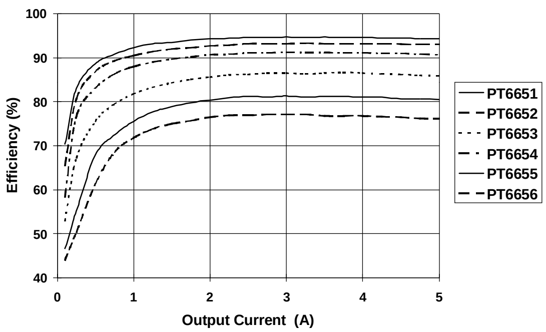
Specifications (Unless otherwise stated, T_a =25 °C, V_{in} =24 V, C_{in} =560 µF, C_{out} =330 µF, and I_o =$I_o$max)

Characteristic	Symbol	Conditions		PT6650 SERIES Min	Typ	Max	Units
Output Current	I_o	Over V_{in} range	V_o ≤12 V V_o =15 V	0.1 (1) 0.1 (1)	— —	5 (2) 4 (2)	A
Input Voltage Range	V_{in}	I_o(min) ≤ I_o ≤ I_o(max)	V_o < 6 V V_o > 6 V	9 V_o + 3	— —	28 28	V
Output Voltage Tolerance	ΔV_o	Over V_{in} range T_a = –40 °C to 65 °C		V_o–0.1	—	V_o+0.1	V
Output Voltage Adjust Range	V_o adj	Pin 14 to V_o or ground	V_o = 3.3 V V_o = 2.5 V V_o = 5 V V_o = 9 V V_o = 12 V V_o = 15 V	2.2 1.8 3 6 9 10	— — — — — —	4.7 4.3 6.5 10.2 13.6 17	V
Line Regulation	Reg_{line}	9 V ≤ V_{in} ≤ 28 V		—	±0.5	±1	%V_o
Load Regulation	Reg_{load}	0.1 ≤ I_o ≤5 A		—	±0.5	±1	%V_o
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth	V_o < 6 V V_o > 6 V	— —	50 1	— —	mV_{pp} %V_o
Transient Response	t_{tr}	0.15 A/µs load step, 50% to 100% $I_o$max		—	100	—	µSec
with C2 = 330µF	V_{tr}	V_o over/undershoot		—	100	—	mV
Efficiency	η	I_o =50 % I_o max	V_o = 3.3 V V_o = 2.5 V V_o = 5 V	— — —	81 76 85	— — —	%
		I_o = I_o max	V_o = 3.3 V V_o = 2.5 V V_o = 5 V	— — —	80 75 84	— — —	%
Switching Frequency	f_s	9 V ≤ V_{in} ≤ 28 V		500	550	600	kHz
On/Off Standby (Pin 3) Input High Voltage Input Low Voltage	 V_{IH} V_{IL}	Referenced to GND		 1 –0.1	 — —	 Open (3) 0.3	V
Input Low Current	I_{IL}			—	–0.25	–	mA
Standby Input Current	I_{in} standby	pin 3 to GND		—	15	30	mA
External Output Capacitance	C_{out}			330	—	3,000	µF
External Input Capacitance	C_{in}			560 (4)	—	—	µF
Operating Temperature Range	T_a	Over V_{in} range		–40	—	85 (2)	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module pins or case		—	—	215 (5)	°C
Storage Temperature	T_s	—		–40	—	125	°C
Reliability	MTBF	Per Bellcore TR-332 50% stress, T_a =40 °C, ground benign		7.2	—	—	10^6 Hrs
Mechanical Shock	—	Per Mil-Std-883D, method 2002.3, 1ms, half-sine, mounted to a fixture		—	500	—	G's
Mechanical Vibration	—	Mil-Std-883D, Method 2007.2, 20-2000Hz, soldered in PCB		—	7.5	—	G's
Weight	—		Case styles P, D, & E Case styles R, G, & B Case styles L & M Case styles F & Q	— — — —	12.5 16.5 15.5 22	— — — —	grams
Flammability	—	Materials meet UL 94V-0					

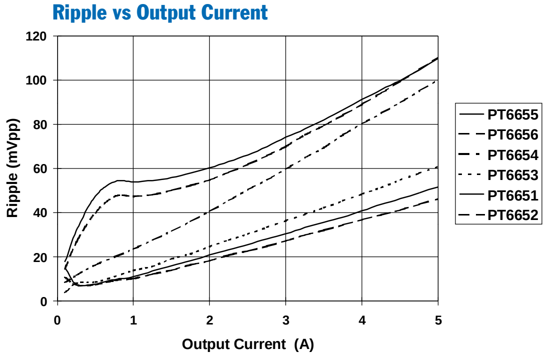
Notes: *(1) The ISR will operate at no load with reduced specifications.*
(2) See Safe Operating Area curves or contact the factory for the appropriate derating.
(3) The STBY control (pin 3) has an internal pull-up and if it is left open circuit the module will operate when input power is applied. The open-circuit voltage is typcially 1.5 V. Consult the related application note for other interface considerations.*
(4) The module requires a 560µF electrolytic capacitor at the input and 330µF at the output for proper operation in all applications. In addition, the input capacitance, Cin, must be rated for a minimum of 1.2 Arms of ripple current. For transient or dynamic load applications additional capacitance may be necessary. For more information consult the related application note on capacitor recommendations.
(5) During solder reflow of SMD package version do not elevate the module case, pins, or internal component temperatures above a peak of 215°C. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products," (SLTA051).

PT6650 Series @V_{IN}= 24 V (See Note A)

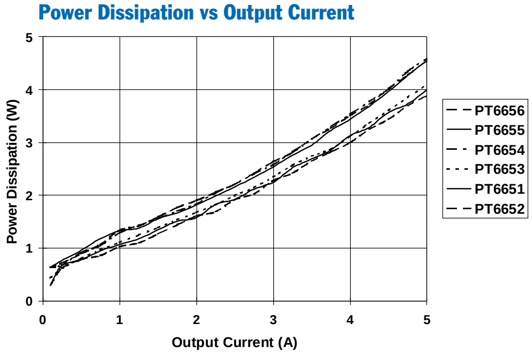
Efficiency vs Output Current



Ripple vs Output Current

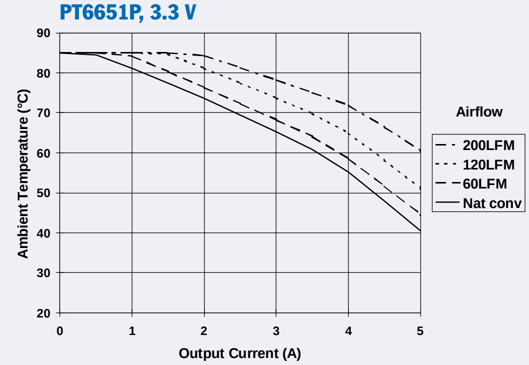


Power Dissipation vs Output Current

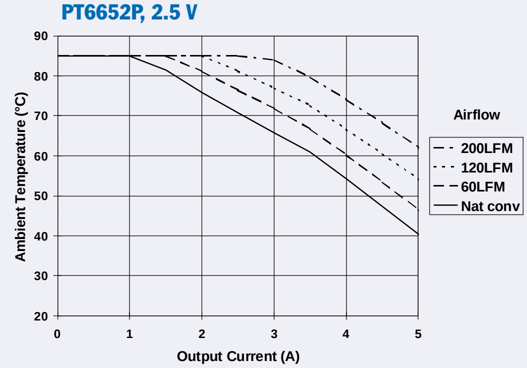


Safe Operating Area @V_{IN}= 24 V (See Note B)

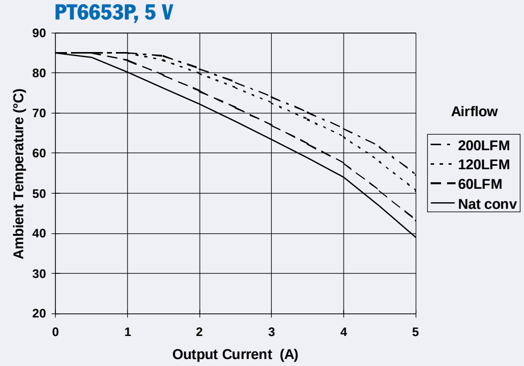
PT6651P, 3.3 V



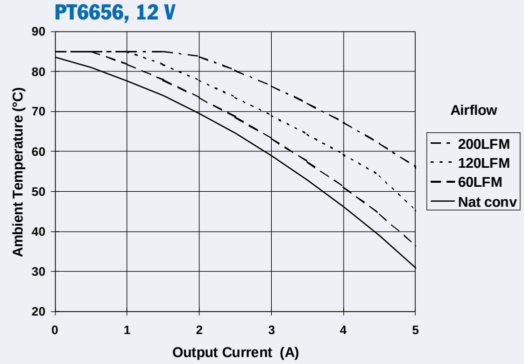
PT6652P, 2.5 V



PT6653P, 5 V



PT6656, 12 V



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the regulator.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures*

Capacitor Recommendations for the PT6650 Regulator Series

Input Capacitor:
The required input capacitor is determined by 560 µF capacitance value, and a minimum ripple current rating of 1.2 Arms. The ripple current rating and less than 120 mΩ equivalent series resistance (ESR) are the major considerations, along with operating temperature, when selecting input capacitors.

Tantalum/Os-Con capacitors are not recommended due to a minimum voltage rating of 2× (the max. DC voltage + AC ripple). This is standard practice to ensure reliability.

Output Capacitors:
The ESR specification of the output capacitor should be a minimum of 50 mΩ *. Electrolytic capacitors have marginal ripple performance at frequencies greater than 400 kHz but excellent low frequency transient response. Above the ripple frequency ceramic capacitors are necessary to improve the transient response and reduce any high-frequency noise components apparent during higher current excursions. Electrolytic capacitors with appropriate ESR values are identified in Table 1-1. In low-temperature applications (<0 °C), a higher capacitance with lower ESR will improve performance.

** Os-Con and ultra low ESR type capacitors are not recommended on the output bus as they degrade regulator stability.*

Tantalum Capacitors (For V_o <5.1 V)
Tantalum type capacitors can be used on the output bus for output voltages less than 5.1 V. Voltages higher than this will exceed the capacitor's published surge voltage limits.

If tantalum capacitors are located on the output bus, an appropriate fuse with I^2t current derating is recommended along with an external clamp component. An Output Over-voltage Clamp (OOVC) will fault the output fuse to protect the capacitors in event of an over-voltage condition. The OOVC can be a simple zener high power diode, 3 W to 5 W, located on the load side of the output bus. The zener diode should be rated to 1.3 times the normal output voltage.

Capacitor Table
Table 1-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (Equivalent Series Resistance at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Table 1-1: Input/Output Capacitors

Capacitor Vendor/ Series	Capacitor Characteristics					Quantity		
	Working Voltage	Value (µF)	(ESR) Equivalent Series Resistance	Max. Ripple Current @85°C (Irms)	Physical Size (mm)	Input Bus	Output Bus	Vendor Part Number
Panasonic FC (Radial)	50 V 50 V 50 V	560 390 390	0.068 Ω 0.080 Ω 0.080 Ω	1900 mA 1610 mA 1610 mA	18×15 16×15 16×15	1 2 2	1 1 1	EEUFC1H561 EEUFC1H391S EEUFC1H391S
FC/FK (SMT)	63 V 35 V 50 V	680 330 1000	0080 Ω 0.080 Ω 0.073 Ω	1690 mA 850 mA 1610 mA	18×16.5 10×10.2 16×16.5	1 N/R [1] 1	1 1 1	EEVFK1J681M EEVFK1V331P EEVFK1H102M
United Chemi-con LXZ/LXV Series	50 V 35 V	680 330	0.048 Ω 0.068 Ω	1840 mA 1050 mA	16×20 10×16	1 N/R [1]	1 1	LXZ50VB681M16X20LL LXV35VB331M10X16LL
MVY (SMT)	35 V	220	0.150 Ω	670 mA	10×10.3	N/R [1]	2	MVY35VC2211M10X10TP
Nichicon PM Series	50 V 63 V 50 V	560 560 330	0.044 Ω 0.039 Ω 0.060 Ω	1550 mA 1400 mA 1210 mA	16×20 18×20 16×15	1 1 2	1 1 1	UPM1H561MHH6 UPM1J561MHH6 UPM1H331MHH6
AVX Tantalum TPS (SMT)	10 V 10 V	330 330	0.10 Ω 0.06 Ω	>2500 mA >3000 mA	7.3L ×5.7W ×4.1H	N/R [1] N/R [1]	1 [2] 1 [2]	TPSE337M010R0100 (V_o <5.1V) TPSV337M010R0060 (V_o <5.1V)
Kemet Tantalum T496 /T495 Series (SMT)	10 V 10 V	220 220	0.500 Ω 0.070 Ω	500 mA >2000 mA	4.3W ×7.3L ×4.0H	N/R [1] N/R [1]	2 [2] 2 [2]	T496X227M010AS (V_o <5.1V) T495X227M0100AS (V_o <5.1V)
Sprague Tantalum 594D Series (SMT)	10 V	330	0.130 Ω	1393 mA	7.2L ×6W ×4.1H	N/R [1]	1 [2]	595D337X0010R2T (V_o <5.1V)

Notes: [1] N/R –Not recommended. The voltage rating does not meet the minimum operating limits.
[2] A fused input bus is recommended when tantalum capacitors are used on the output bus.

Using the Standby Function on the PT6650 Series of 12/24-V Input Bus Converters

For applications requiring output voltage On/Off control, the 14-pin PT6650 ISR series incorporates a standby function. This feature may be used for power-up/shutdown sequencing, and wherever there is a requirement for the output status of the module to be controlled by external circuitry.

The standby function is provided by the *STBY** control, pin 3. If pin 3 is left open-circuit the regulator operates normally, providing a regulated output whenever a valid supply voltage is applied to V_{in} (pins 4, 5, & 6) with respect to GND (pins 7-10). Connecting pin 3 to ground [1] will disable the regulator output and reduce the input current to less than 30 mA [3]. Grounding the standby control will also hold-off the regulator output during the period that input power is applied.

The standby input is ideally controlled with an open-drain discrete transistor (See Figure 2-1). It can also be driven directly from a dedicated TTL [2] compatible gate. Table 2-1 provides details of the threshold requirements.

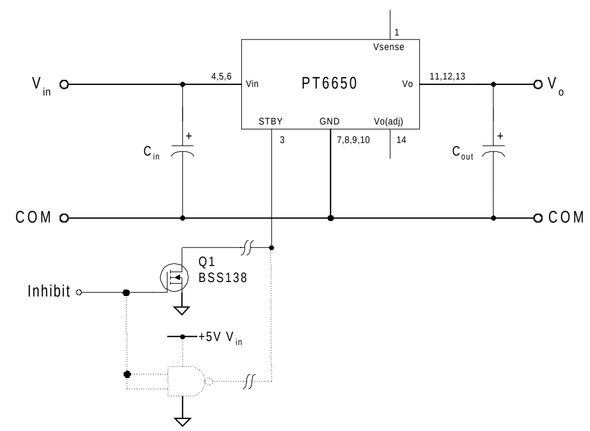
Table 2-1 Inhibit Control Thresholds [1, 2]

Parameter	Min	Max
Enable (V_{IH})	1 V	5 V
Disable (V_{IL})	–0.1 V	0.3 V

Notes:

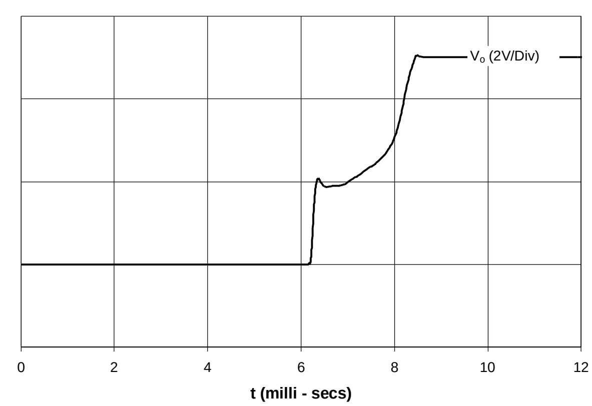
1. The Standby input on the PT6650 regulator series may be controlled using either an open-collector (or open-drain) discrete transistor, or a device with a totem-pole output. A pull-up resistor is not necessary. The control input has an open-circuit voltage of about 1.5 Vdc. To disable the regulator output, the control pin must be “pulled” to less than 0.3 Vdc with a low-level 0.25 mA maximum sink to ground.
2. The Standby input on the PT6650 series is also compatible with TTL logic. A standard TTL logic gate will meet the 0.3 V V_{IL}(max) requirement (Table 2-1) at 0.25 mA sink current. *Do not* drive the Standby control input above 5 Vdc.
3. When the regulator output is disabled the current drawn from the input source is reduced to approximately 15 mA (30 mA maximum).
4. The turn-off time of Q_1, or rise time of the standby input is not critical on the PT6650 series. Turning Q_1 off over periods up to 100 ms will not damage the regulator. However, a slow turn-off time will increase both the initial delay and rate-of-rise of the output voltage.

Figure 2-1



Turn-On Time: Turning Q_1 off in Figure 2-1, removes the low-voltage signal at pin 3 and enables the output. The PT6650 series of regulators will provide a fully regulated output voltage within 12 ms. The actual turn-on time may vary with load and the total amount of output capacitance. Figure 2-2 shows the typical output voltage waveform of a PT6653 (5 V) following the prompt turn-off of Q_1 at time t =0 secs. The waveform was measured with a 24 V input voltage, and 5 A resistive load.

Figure 2-2



Adjusting the Output Voltage of the PT6650 5-A 24-V Bus Converter Series

The output voltage of the PT6650 Series ISRs may be adjusted higher or lower than the factory trimmed pre-set voltage with the addition of a single external resistor. Table 3-1 gives the allowable adjustment range for each model in the series as V_a (min) and V_a (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor R_2, between pin 14 (V_o adj) and pins 7-10 (GND).

Adjust Down: To decrease the output voltage, add a resistor (R_1), between pin 14 (V_o adj) and pins 11-13 (V_{out}).

Refer to Figure 3-1 and Table 3-2 for both the placement and value of the required resistor, either (R_1) or R_2 as appropriate.

Notes:

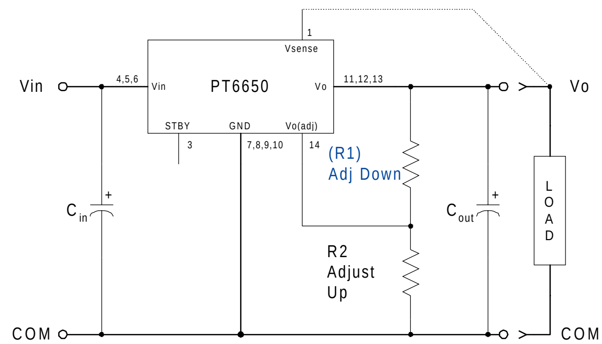
1. Use only a single 1 % resistor in either the (R_1) or R_2 location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from V_o adjust to either *GND*, *V_{out}*, or the *Remote Sense* pin. Any capacitance added to the V_o adjust pin will affect the stability of the ISR.
3. If the remote sense feature is being used, connecting the resistor (R_1) between pin 14 (V_o adj) and pin 1 (Remote Sense) can benefit load regulation.
4. Adjustments to the output voltage may place additional limits on the input voltage for the part. The revised limits must comply with the following requirements.

   V_{in} (min) = (V_{out} + 3) V or 9 V, whichever is higher.

   V_{in} (max) = (10 x V_{out}) V or 28 V, whichever is less.

5. For output voltages above 12.5 Vdc, the maximum output current must be limited to 4 Adc.

Figure 3-1



The values of (R_1) [adjust down], and R_2 [adjust up], can also be calculated using the following formulae.

$$(R_1) = \frac{R_o (V_o - 1.25)(V_a - 1.25)}{1.25 (V_o - V_a)} - R_s \quad \text{k}\Omega$$

$$R_2 = \frac{R_o (V_o - 1.25)}{V_a - V_o} - R_s \quad \text{k}\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
R_o = The resistance value in Table 3-1
R_s = The series resistance from Table 3-1

Table 3-1

PT6650 ADJUSTMENT AND FORMULA PARAMETERS

Series Pt #	PT6652	PT6651	PT6653	PT6654	PT6656	PT6655
V_o (nom)	2.5 V	3.3 V	5 V	9 V	12 V	15 V
V_a (min)	1.8 V	2.2 V	3 V	6 V	9 V	10 V
V_a (max)	4.3 V	4.7 V	6.5 V	10.2 V	13.6 V	17 V
R_o (kΩ)	4.99	4.22	2.49	2	2	2
R_s (kΩ)	2.49	4.99	4.99	12.7	12.7	12.7

Table 3-2

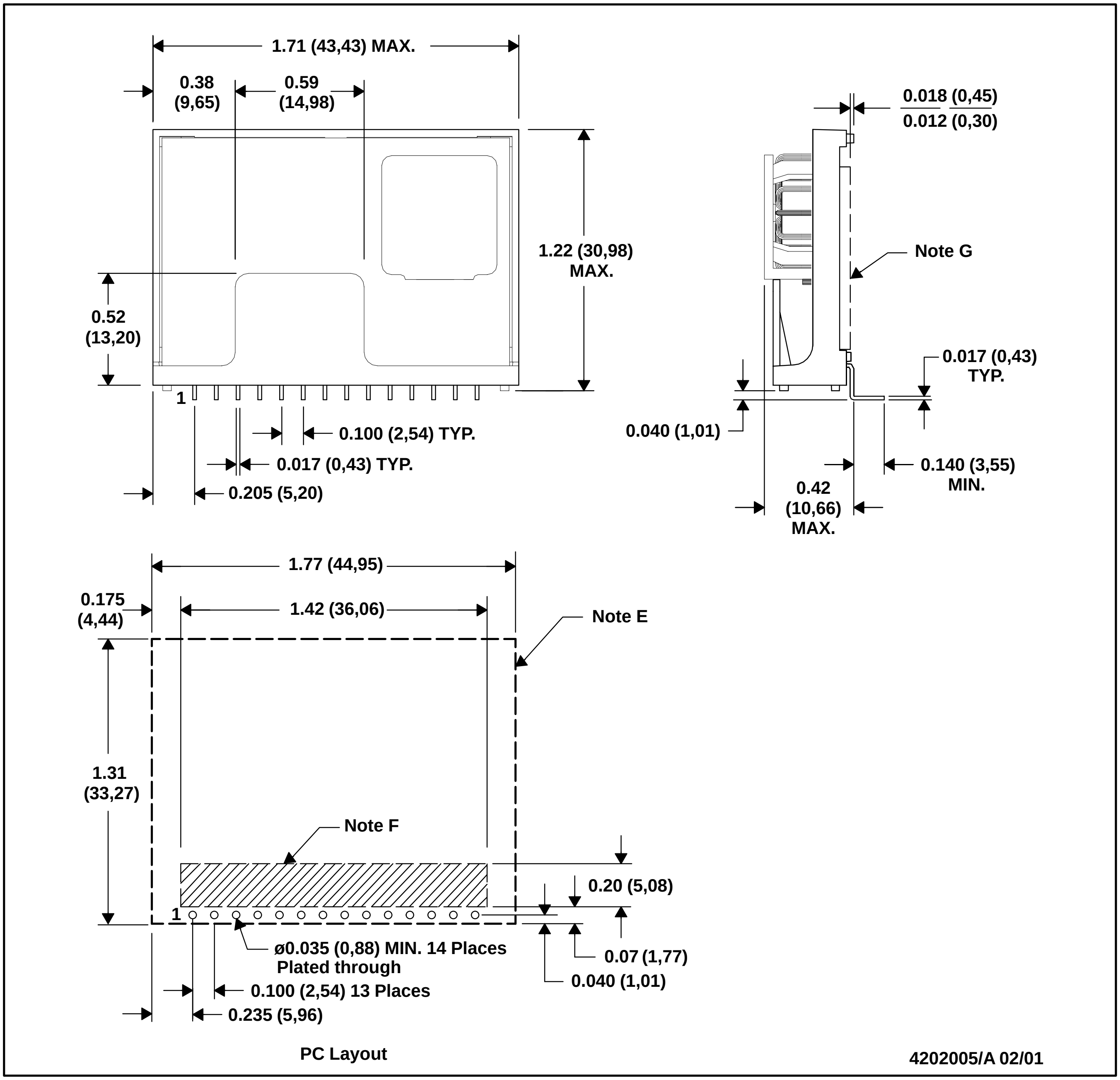
PT6650 ADJUSTMENT RESISTOR VALUES

Series Pt #	PT6652	PT6651	PT6653
Current	5 Adc	5 Adc	5A dc
V_o (nom)	2.5 Vdc	3.3 Vdc	5 Vdc
V_a (req'd)			
1.8	(1.4) kΩ		
1.9	(2.9) kΩ		
2.0	(5.0) kΩ		
2.1	(8.1) kΩ		
2.2	(13.3) kΩ	(1.0) kΩ	
2.3	(23.7) kΩ	(2.3) kΩ	
2.4	(54.9) kΩ	(3.9) kΩ	
2.5		(5.8) kΩ	
2.6	59.9 kΩ	(8.4) kΩ	
2.7	28.7 kΩ	(11.7) kΩ	
2.8	18.3 kΩ	(16.5) kΩ	
2.9	13.1 kΩ	(23.6) kΩ	
3.0	10.0 kΩ	(35.4) kΩ	(1.6) kΩ
3.1	7.9 kΩ	(59.0) kΩ	(2.3) kΩ
3.2	6.4 kΩ	(130.0) kΩ	(3.1) kΩ
3.3	5.3 kΩ		(4.0) kΩ
3.4	4.4 kΩ	81.5 kΩ	(5.1) kΩ
3.5	3.8 kΩ	38.3 kΩ	(6.2) kΩ
3.6	3.2 kΩ	23.8 kΩ	(7.6) kΩ
3.7	2.7 kΩ	16.6 kΩ	(9.1) kΩ
3.8	2.3 kΩ	12.3 kΩ	(10.9) kΩ
3.9	2.0 kΩ	9.4 kΩ	(13.0) kΩ
4.0	1.7 kΩ	7.4 kΩ	(15.6) kΩ
4.1	1.4 kΩ	5.8 kΩ	(18.7) kΩ
4.2	1.2 kΩ	4.6 kΩ	(22.6) kΩ
4.3	1.0 kΩ	3.7 kΩ	(27.6) kΩ
4.4		2.9 kΩ	(34.2) kΩ
4.5		2.2 kΩ	(43.6) kΩ
4.6		1.7 kΩ	(57.6) kΩ
4.7		1.2 kΩ	(80.9)kΩ
4.8			(128.0) kΩ
4.9			(268.0) kΩ
5.0			
5.1			88.4 kΩ
5.2			41.7 kΩ
5.3			26.1 kΩ
5.4			18.4k Ω
5.5			13.7 kΩ
5.6			10.6 kΩ
5.7			8.4 kΩ
5.8			6.7 kΩ
5.9			5.4 kΩ
6.0			4.4 kΩ
6.1			3.5 kΩ
6.2			2.8 kΩ
6.3			2.2 kΩ
6.4			1.7 kΩ
6.5			1.2 kΩ

Series Pt #	PT6654	PT6656	PT6655
Current	5 Adc	5 Adc	4 Adc
V_o (nom)	9 Vdc	12 Vdc	15 Vdc
V_a (req'd)			
6.0	(6.9) kΩ		
6.2	(9.2) kΩ		
6.4	(11.9) kΩ		
6.6	(14.0) kΩ		
6.8	(18.6) kΩ		
7.0	(23.0) kΩ		
7.2	(28.3) kΩ		
7.4	(35.0) kΩ		
7.6	(43.5) kΩ		
7.8	(55.0) kΩ		
8.0	(71.0) kΩ		
8.2	(95.0) kΩ		
8.4	(135.0) kΩ		
8.6	(215.0) kΩ		
8.8	(455.0) kΩ		
9.0		(31.7) kΩ	
9.2	64.8 kΩ	(36.1) kΩ	
9.4	26.1 kΩ	(41.2) kΩ	
9.6	13.1 kΩ	(47.1) kΩ	
9.8	6.7 kΩ	(54.1) kΩ	
10.0	2.8 kΩ	(62.6) kΩ	(25.8) kΩ
10.2	0.2 kΩ	(72.8) kΩ	(28.3) kΩ
10.4		(85.7) kΩ	(31.1) kΩ
10.6		(102.0) kΩ	(34.1) kΩ
10.8		(124.0) kΩ	(37.3) kΩ
11.0		(155.0) kΩ	(40.9) kΩ
11.2		(201.0) kΩ	(44.9) kΩ
11.4		(278.0) kΩ	(49.3) kΩ
11.6		(432.0) kΩ	(54.3) kΩ
11.8		(895.0) kΩ	(59.8) kΩ
12.0			(66.1) kΩ
12.2		94.8 kΩ	(73.3) kΩ
12.4		41.1 kΩ	(81.6) kΩ
12.6		23.1 kΩ	(91.3) kΩ
12.8		14.2 kΩ	(103.0) kΩ
13.0		8.8 kΩ	(117.0) kΩ
13.2		5.2 kΩ	(133.0) kΩ
13.4		2.7 kΩ	(154.0) kΩ
13.6		0.7 kΩ	(181.0) kΩ
13.8			(217.0) kΩ
14.0			(268.0) kΩ
14.2			(343.0) kΩ
14.5			(570.0) kΩ
15.0			
15.5			42.3 kΩ
16.0			14.8 kΩ
16.5			5.6 kΩ
17.0			1.1 kΩ

R_1 = (Blue) R_2 = Black

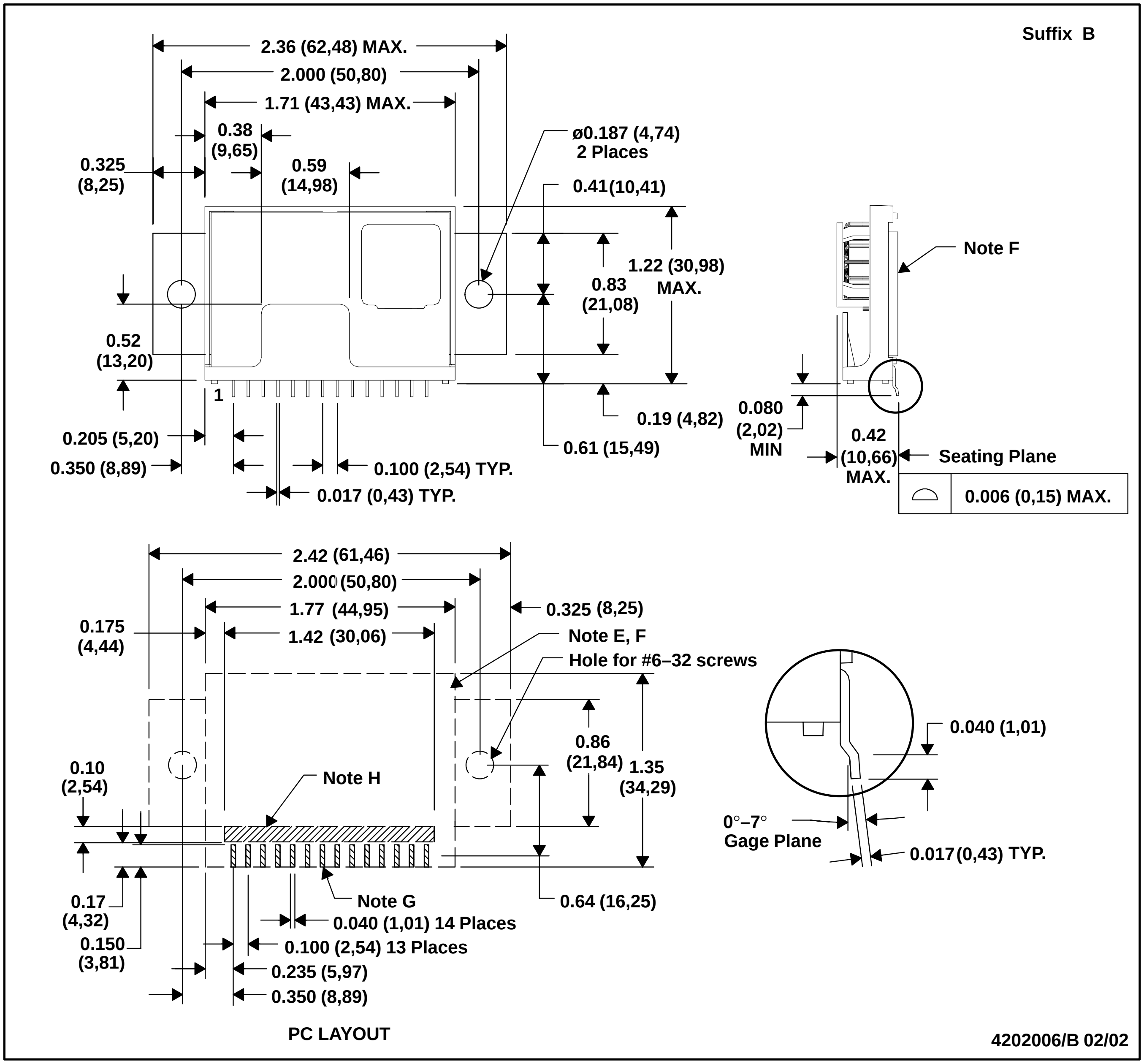
EEA (R–PSIP–T14) **PLASTIC SINGLE-IN-LINE MODULE**



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2-place decimals are ± 0.030 (± 0, 76 mm).
- D. 3-place decimals are ± 0.010 (± 0, 25 mm).
- E. Recommended mechanical keep-out area.
- F. No copper, power or signal traces in this area.
- G. D-suffix parts include a metal heat spreader. No signal traces are allowed under the heat spreader area. A solid copper island is recommended, which may be grounded. A-suffix does not include a metal heat spreader.

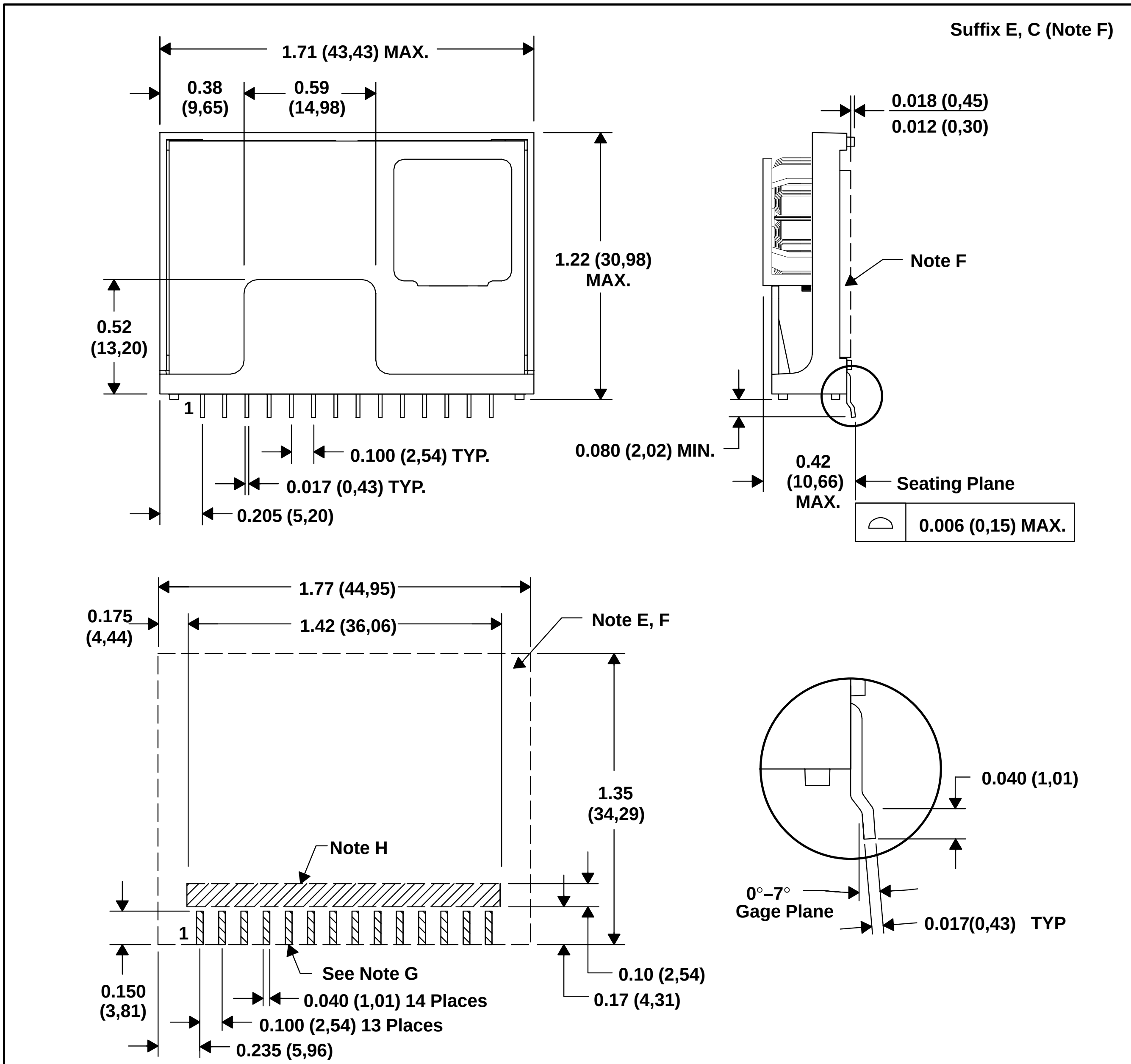
MPSI014A – MARCH 2001 – REVISED FEBRUARY 2002

EEK (R–PSIP–G14) **PLASTIC SINGLE-IN-LINE MODULE**



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2–place decimals are ± 0.030 (± 0,76 mm).
- D. 3–place decimals are ± 0.010 (± 0,25 mm).
- E. Recommended mechanical keep-out area.
- F. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded.
- G. Power pin connections should utilize two or more vias per input, ground and output pin.
- H. No copper, power or signal traces in this area.

EEC (R–PSIP–G14) PLASTIC SINGLE-IN-LINE MODULE

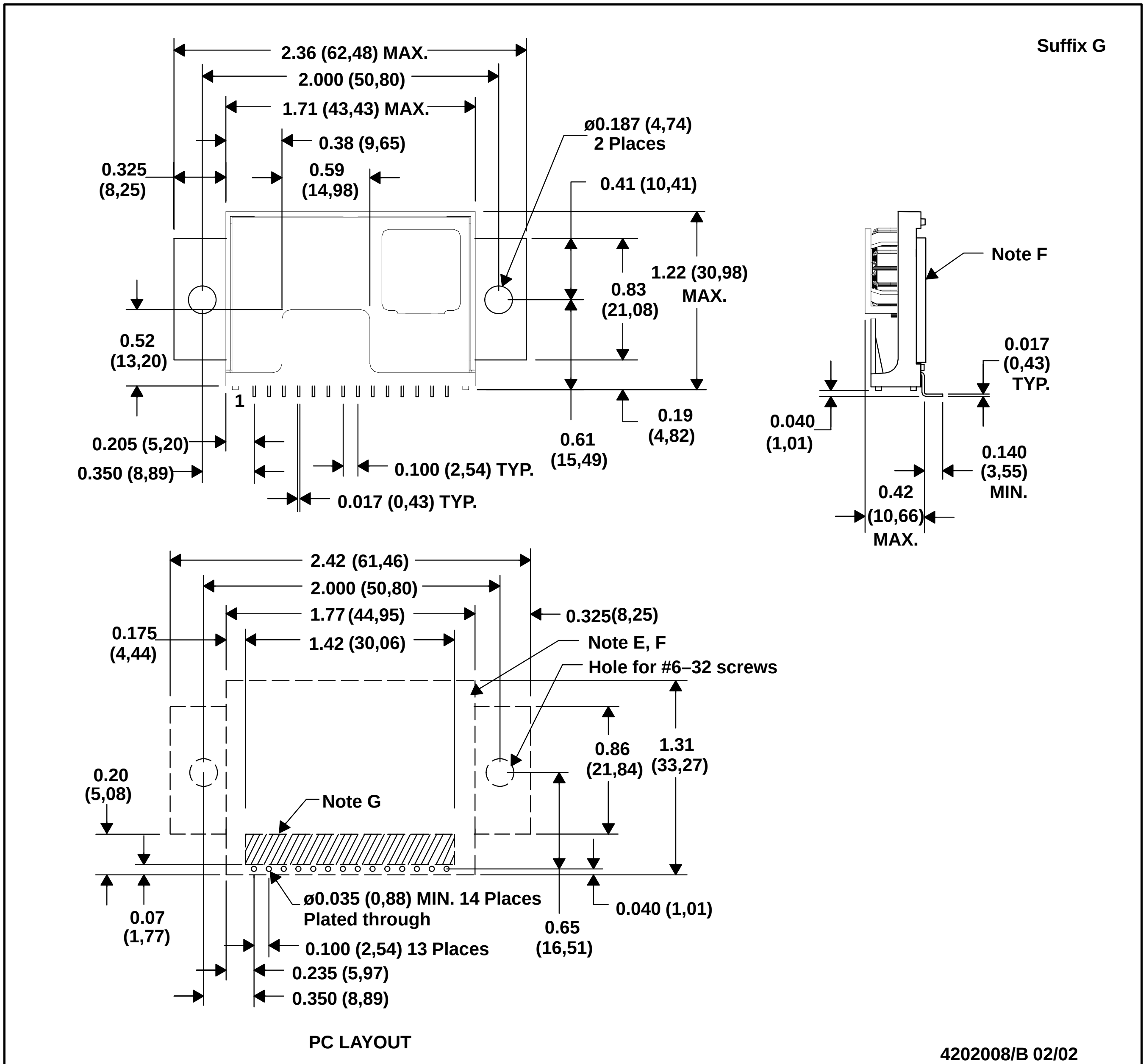


PC LAYOUT

4202007/B 12/01

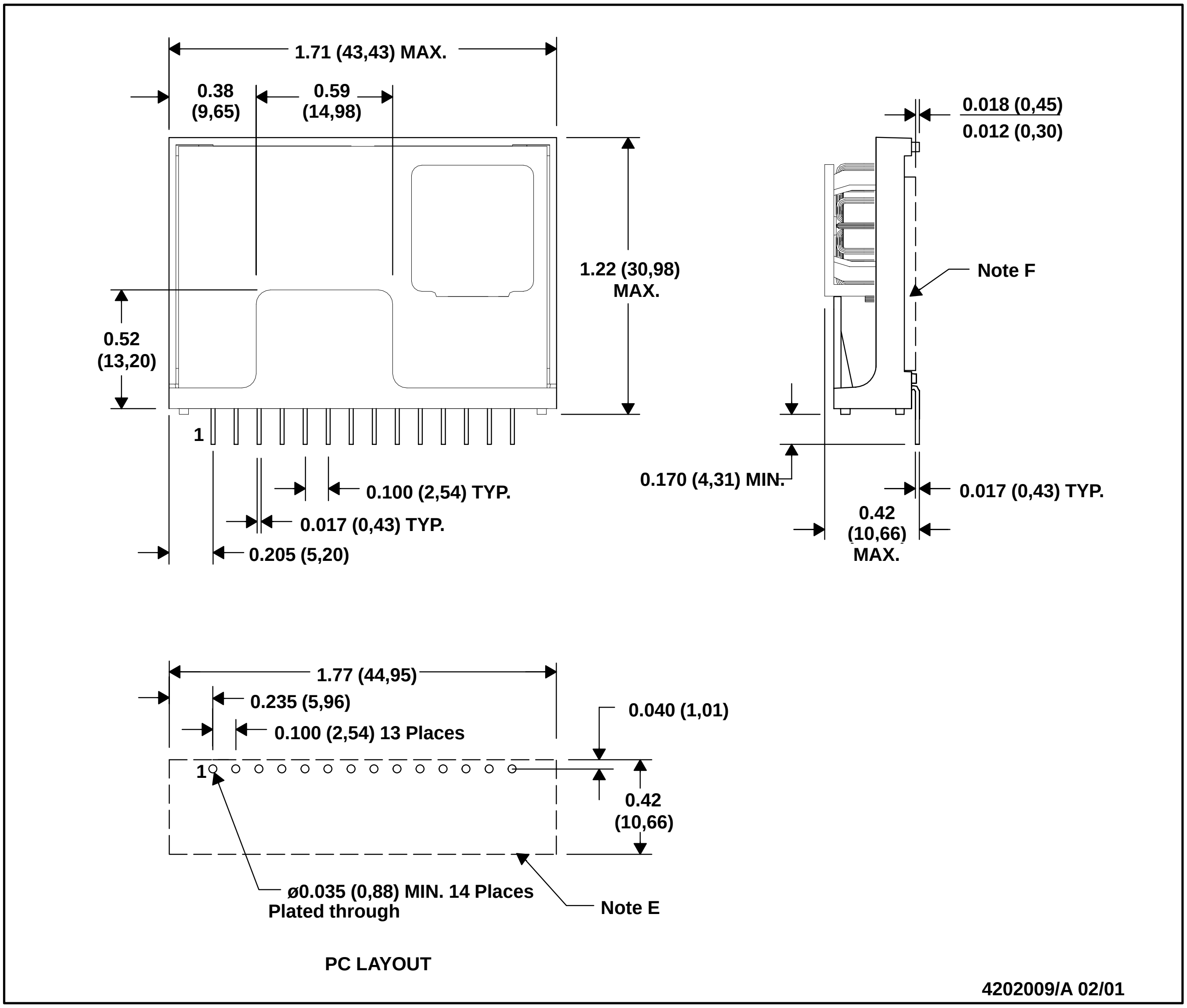
NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2–place decimals are ± 0.030 (± 0, 76 mm).
- D. 3–place decimals are ± 0.010 (± 0, 25 mm).
- E. Recommended mechanical keep-out area.
- F. E-suffix parts include a metal heat spreader. No signal traces are allowed under the heat spreader area. A solid copper island is recommended, which may be grounded. C-suffix does not include a metal heat spreader.
- G. Power pin connections should utilize two or more vias per input, ground and output pin.
- H. No copper, power or signal traces in this area.

EEG (R–PSIP–T14) **PLASTIC SINGLE-IN-LINE MODULE**



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2-place decimals are ± 0.030 (± 0,76 mm).
- D. 3-place decimals are ± 0.010 (± 0,25 mm).
- E. Recommended mechanical keep-out area.
- F. The metal tab is isolated but electrically conductive.
  No signal traces are allowed under the metal tab area.
  A solid copper island is recommended, which may be grounded.
- G. No copper, power or signal traces in this area.

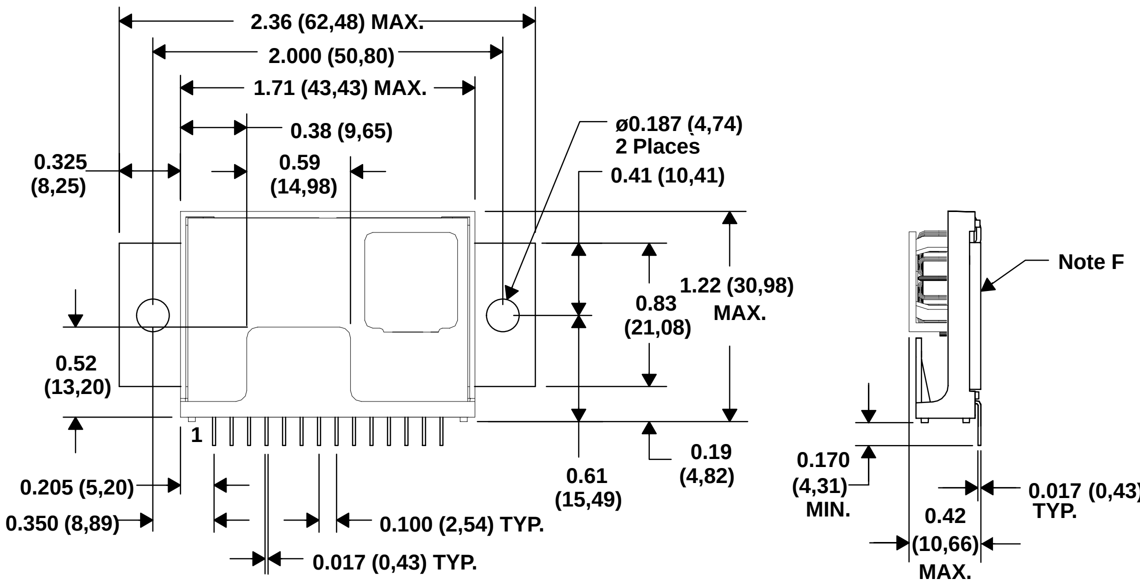
EED (R–PSIP–T14) **PLASTIC SINGLE-IN-LINE MODULE**

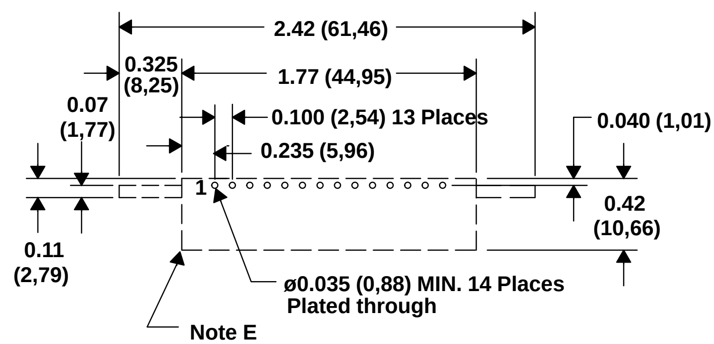


NOTES: A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2-place decimals are ± 0.030 (± 0, 76 mm).
D. 3-place decimals are ± 0.010 (± 0, 25 mm).
E. Recommended mechanical keep-out area.
F. P-suffix parts include a metal heat spreader.
The heat spreader is isolated but electrically
conductive, it can be grounded.
N-suffix does not include a metal heat spreader.

EEE (R–PSIP–T14) **PLASTIC SINGLE-IN-LINE MODULE**

Suffix R



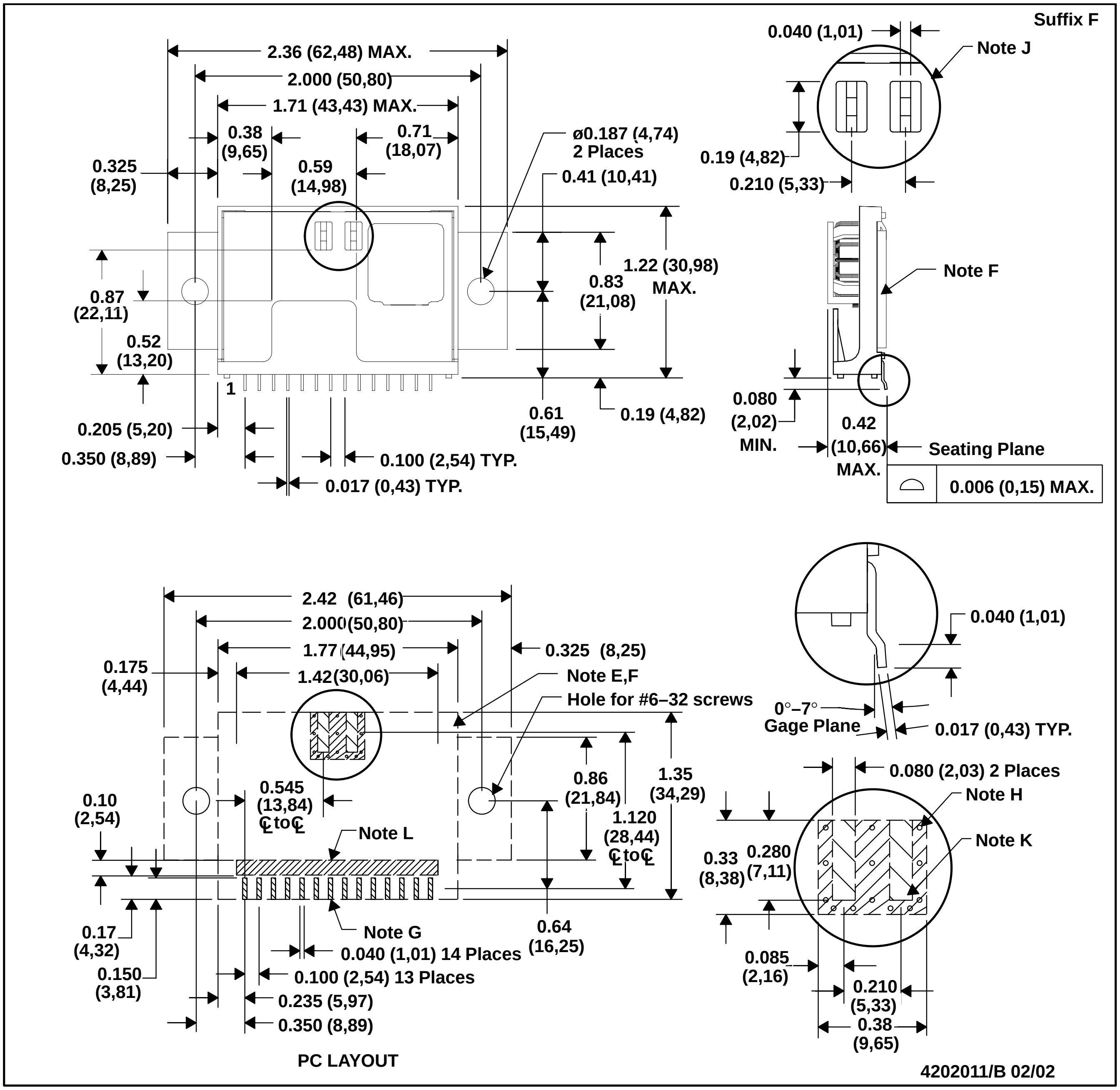


PC LAYOUT

4202010/B 02/02

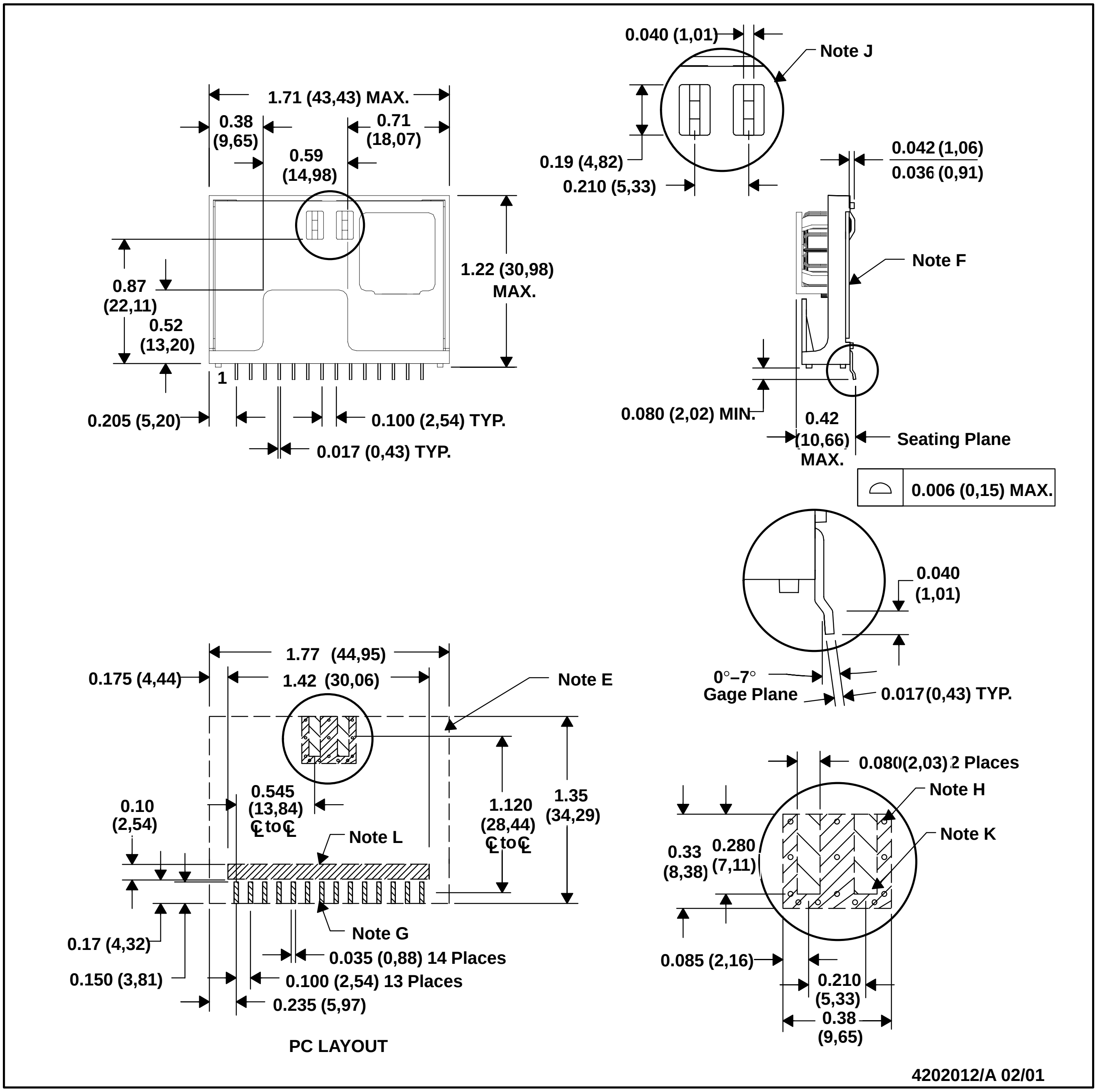
NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2-place decimals are ± 0.030 (± 0,76 mm).
- D. 3-place decimals are ± 0.010 (± 0,25 mm).
- E. Recommended mechanical keep-out area.
- F. The metal tab is isolated but electrically conductive, it can be grounded.

EEF (R–PSIP–G14) PLASTIC SINGLE-IN-LINE MODULE



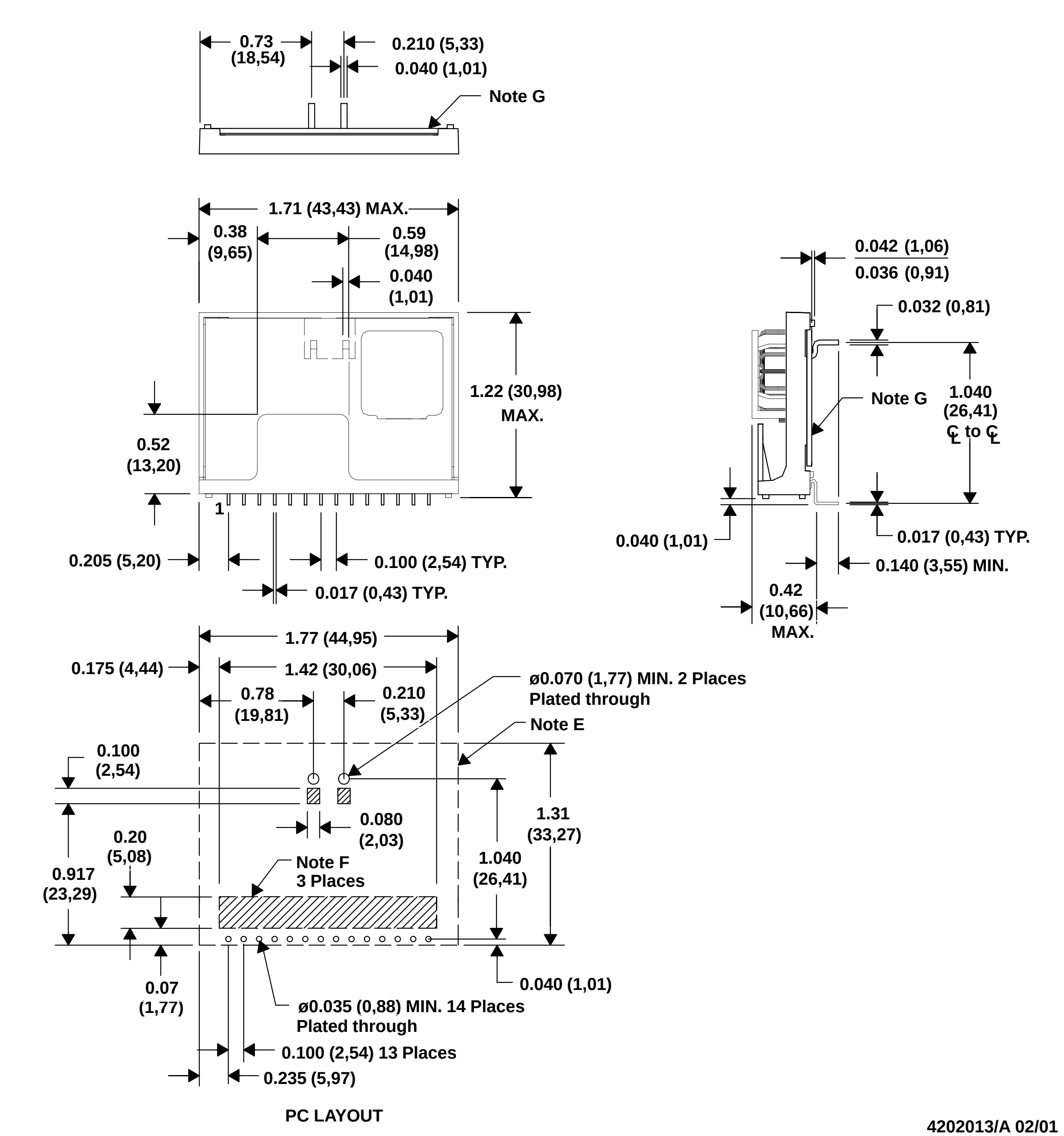
NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2-place decimals are ± 0.030 (± 0, 76 mm).
- D. 3–place decimal are ± 0.010 (± 0, 25 mm).
- E. Recommended mechanical keep-out area.
- F. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded.
- G. Power pin connections should utilize two or more vias per input, ground and output pin.
- H. Minimum copper land area required for solder tab. Vias are recommended to improve copper adhesion or connect land to other ground area.
- J. Underside solder tabs detail.
- K. Solder mask openings to copper island for solder joints to mechanical pins.
- L. No copper, power or signal traces in this area.

EEL (R–PSIP–G14) **PLASTIC SINGLE-IN-LINE MODULE**



NOTES:
- A. All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2–place decimals are ± 0.030 (± 0,76 mm).
- D. 3–place decimals are ± 0.010 (± 0,25 mm).
- E. Recommended mechanical keep-out area.
- F. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded.
- G. Power pin connections should utilize two or more vias per input, ground and output pin.
- H. Minimum copper land area required for solder tab. Vias are recommended to improve copper adhesion or connect land to other ground area.
- J. Underside solder tabs detail
- K. Solder mask openings to copper island for solder joints to mechanical pins.
- L. No copper, power or signal traces in this area.

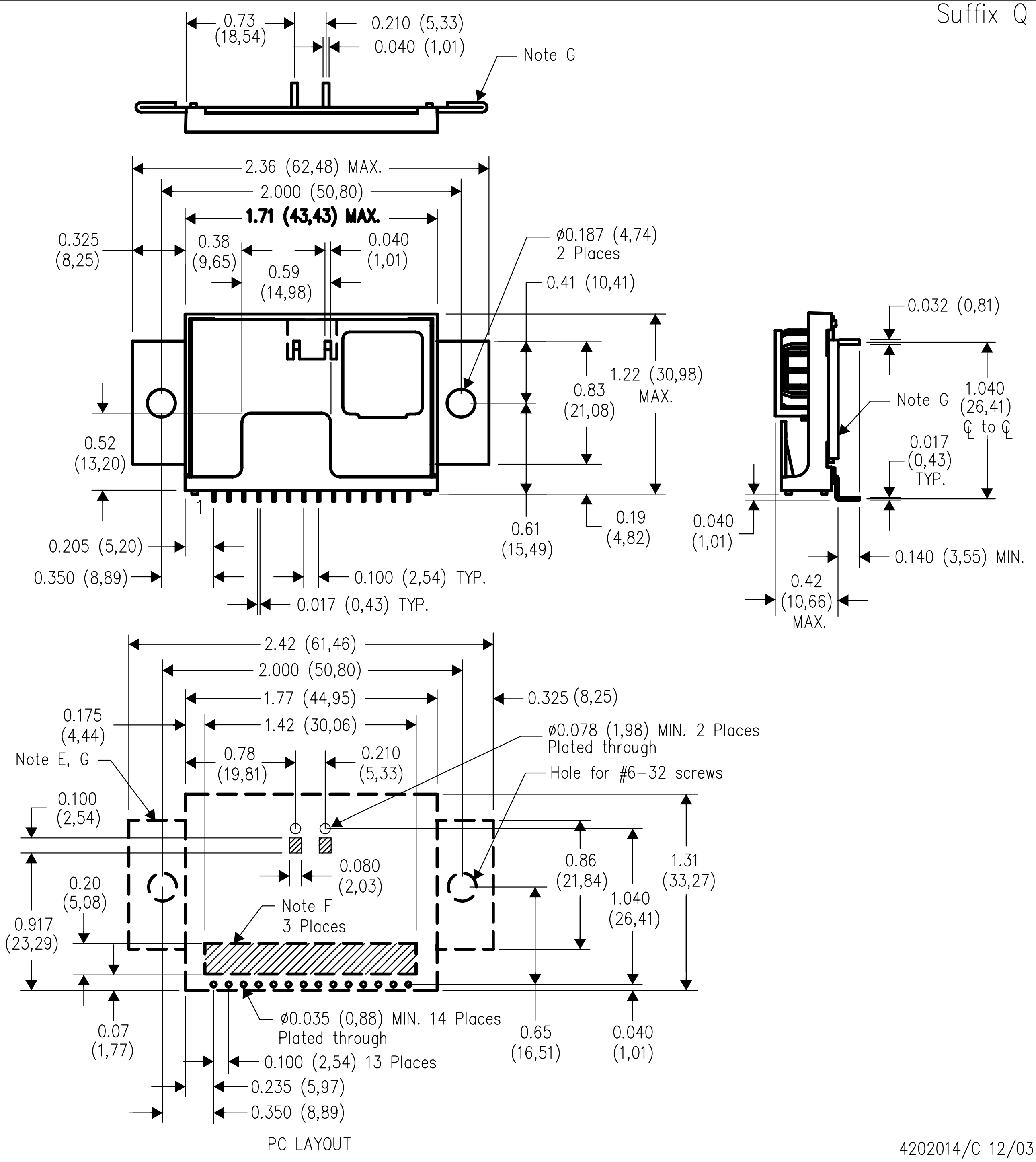
EEM (R–PSIP–T14) **PLASTIC SINGLE-IN-LINE MODULE**



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2-place decimals are ± 0.030 (± 0, 76 mm).
D. 3-place deciamals are ± 0.010 (± 0, 25 mm).
E. Recommended mechanical keep-out area.
F. No copper, power or signal traces in this area.
G. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded to the two underside pins.

EEQ (R–PSIP–T14) PLASTIC SINGLE–IN–LINE MODULE

Suffix Q



4202014/C 12/03

NOTES:

A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended mechanical keep out area.
F. No copper, power or signal traces in this area.
G. The metal tab is isolated but electrically conductive. No signal traces are allowed under the metal tab area. A solid copper island is recommended, which may be grounded to the two underside pins.

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