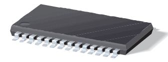

Typical Size
6,4 mm X 9,7 mm

3-V TO 6-V INPUT, 6-A OUTPUT SYNCHRONOUS BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- **30-mΩ, 12-A Peak MOSFET Switches for High Efficiency at 6-A Continuous Output Source or Sink Current**
- **Adjustable Output Voltage Down To 0.9 V With 1.0% Accuracy**
- **Wide PWM Frequency: Fixed 350 kHz, 550 kHz or Adjustable 280 kHz to 700 kHz**
- **Synchronizable to 700 kHz**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Component Count**

APPLICATIONS

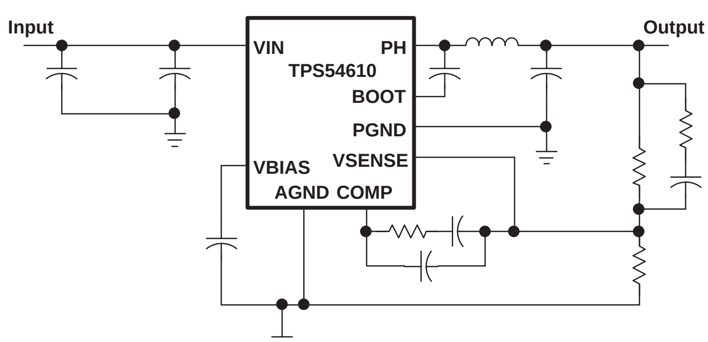
- **Low-Voltage, High-Density Distributed Power Systems**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors**
- **Broadband, Networking and Optical Communications Infrastructure**
- **Portable Computing/Notebook PCs**

DESCRIPTION

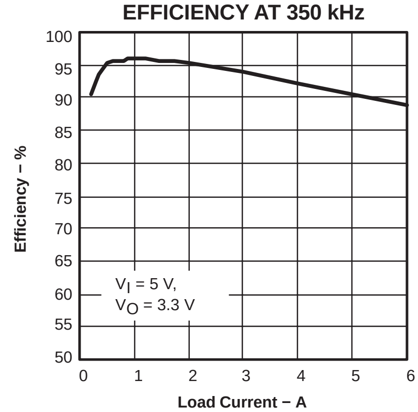
As a member of the SWIFT™ family of dc/dc regulators, the TPS54610 low-input voltage high-output current synchronous buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally or externally set slow-start circuit to limit inrush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

The TPS54610 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

SIMPLIFIED SCHEMATIC



EFFICIENCY AT 350 kHz



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
−40°C to 85°C	Adjustable down to 0.9 V	Plastic HTSSOP (PWP)(1)	TPS54610PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54610PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS54610	UNIT
Input voltage range, V_I	VIN, SS/ENA, SYNC	−0.3 V to 7 V	V
	RT	−0.3 V to 6 V	
	VSENSE	−0.3 V to 4V	
	BOOT	−0.3 V to 17 V	
Output voltage range, V_O	VBIAS, COMP, PWRGD	−0.3 V to 7 V	V
	PH	−0.6 V to 10 V	
Source current, I_O	PH	Internally Limited	
	COMP, VBIAS	6	mA
Sink current, I_S	PH	12	A
	COMP	6	mA
	SS/ENA, PWRGD	10	
Voltage differential	AGND to PGND	±0.3	V
Operating virtual junction temperature range, T_J		−40 to 125	°C
Storage temperature, T_{stg}		−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I	3		6	V
Operating junction temperature, T_J	−40		125	°C

DISSIPATION RATINGS(1)(2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
28 Pin PWP with solder	18.2 °C/W	5.49 W(3)	3.02 W	2.20 W
28 Pin PWP without solder	40.5 °C/W	2.48 W	1.36 W	0.99 W

(1) For more information on the PWP package, refer to TI technical brief, literature number SLMA002.
(2) Test board conditions:
1. 3” x 3”, 4 layers, thickness: 0.062”
2. 1.5 oz. copper traces located on the top of the PCB
3. 1.5 oz. copper ground plane on the bottom of the PCB
4. 0.5 oz. copper ground planes on the 2 internal layers
5. 12 thermal vias (see “Recommended Land Pattern” in applications section of this data sheet)
(3) Maximum power dissipation may be limited by over current protection.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
	Input voltage range, VIN		3.0		6.0	V
$I_{(Q)}$	Quiescent current	f_S = 350 kHz, SYNC ≤ 0.8 V, RT open, PH pin open	11		15.8	mA
		f_S = 550 kHz, SYNC ≥ 2.5 V, RT open, PH pin open	16		23.5	
		Shutdown, SS/ENA = 0 V		1	1.4	
UNDER VOLTAGE LOCK OUT						
	Start threshold voltage, UVLO			2.95	3.0	V
	Stop threshold voltage, UVLO		2.70	2.80		V
	Hysteresis voltage, UVLO		0.14	0.16		V
	Rising and falling edge deglitch, UVLO(1)			2.5		µs
BIAS VOLTAGE						
	Output voltage, VBIAS	$I_{(VBIAS)} = 0$	2.70	2.80	2.90	V
	Output current, VBIAS (2)				100	µA
CUMULATIVE REFERENCE						
V_{ref}	Accuracy		0.882	0.891	0.900	V
REGULATION						
	Line regulation(1)(3)	I_L = 3 A, f_S = 350 kHz, T_J = 85°C			0.04	%/V
		I_L = 3 A, f_S = 550 kHz, T_J = 85°C			0.04	
	Load regulation(1)(3)	I_L = 0 A to 6 A, f_S = 350 kHz, T_J = 85°C			0.03	%/A
		I_L = 0 A to 6 A, f_S = 550 kHz, T_J = 85°C			0.03	
OSCILLATOR						
	Internally set—free running frequency	SYNC ≤ 0.8 V, RT open	280	350	420	kHz
		SYNC ≥ 2.5 V, RT open	440	550	660	
	Externally set—free running frequency range	RT = 180 kΩ (1% resistor to AGND)(1)	252	280	308	kHz
		RT = 100 kΩ (1% resistor to AGND)	460	500	540	
		RT = 68 kΩ (1% resistor to AGND)(1)	663	700	762	
	High level threshold, SYNC		2.5			V
	Low level threshold, SYNC				0.8	V
	Pulse duration, external synchronization, SYNC(1)		50			ns
	Frequency range, SYNC(1)		330		700	kHz
	Ramp valley(1)			0.75		V
	Ramp amplitude (peak-to-peak)(1)			1		V
	Minimum controllable on time(1)				200	ns
	Maximum duty cycle		90%			

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10

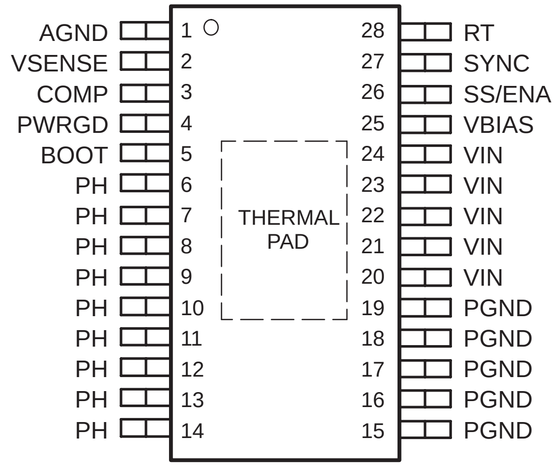
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
	Error amplifier open loop voltage gain	1 kΩ COMP to AGND(1)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(1)	3	5		MHz
	Error amplifier common mode input voltage range	Powered by internal LDO(1)	0		VBIAS	V
	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
	Output voltage slew rate (symmetric), COMP		1.0	1.4		V/µs
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive(1)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, SS/ENA		0.82	1.20	1.40	V
	Enable hysteresis voltage, SS/ENA			0.03		V
	Falling edge deglitch, SS/ENA(1)			2.5		µs
	Internal slow-start time		2.6	3.35	4.1	ms
	Charge current, SS/ENA	SS/ENA = 0 V	3	5	8	µA
	Discharge current, SS/ENA	SS/ENA = 0.2 V, V_I = 2.7 V	2.0	2.3	4.0	mA
POWER GOOD						
	Power good threshold voltage	VSENSE falling		90		$\%V_{ref}$
	Power good hysteresis voltage(1)			3		$\%V_{ref}$
	Power good falling edge deglitch(1)			35		µs
	Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3	V
	Leakage current, PWRGD	V_I = 5.5 V			1	µA
CURRENT LIMIT						
	Current limit trip point	V_I = 3 V Output shorted(1)	7.2	10		A
		V_I = 6 V Output shorted(1)	10	12		
	Current limit leading edge blanking time(1)			100		ns
	Current limit total response time(1)			200		ns
THERMAL SHUTDOWN						
	Thermal shutdown trip point(1)		135	150	165	°C
	Thermal shutdown hysteresis(1)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches	V_I = 6 V(4)		26	47	mΩ
		V_I = 3 V(4)		36	65	

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10
(4) Matched MOSFETs low-side $r_{DS(on)}$ production tested, high-side $r_{DS(on)}$ specified by design

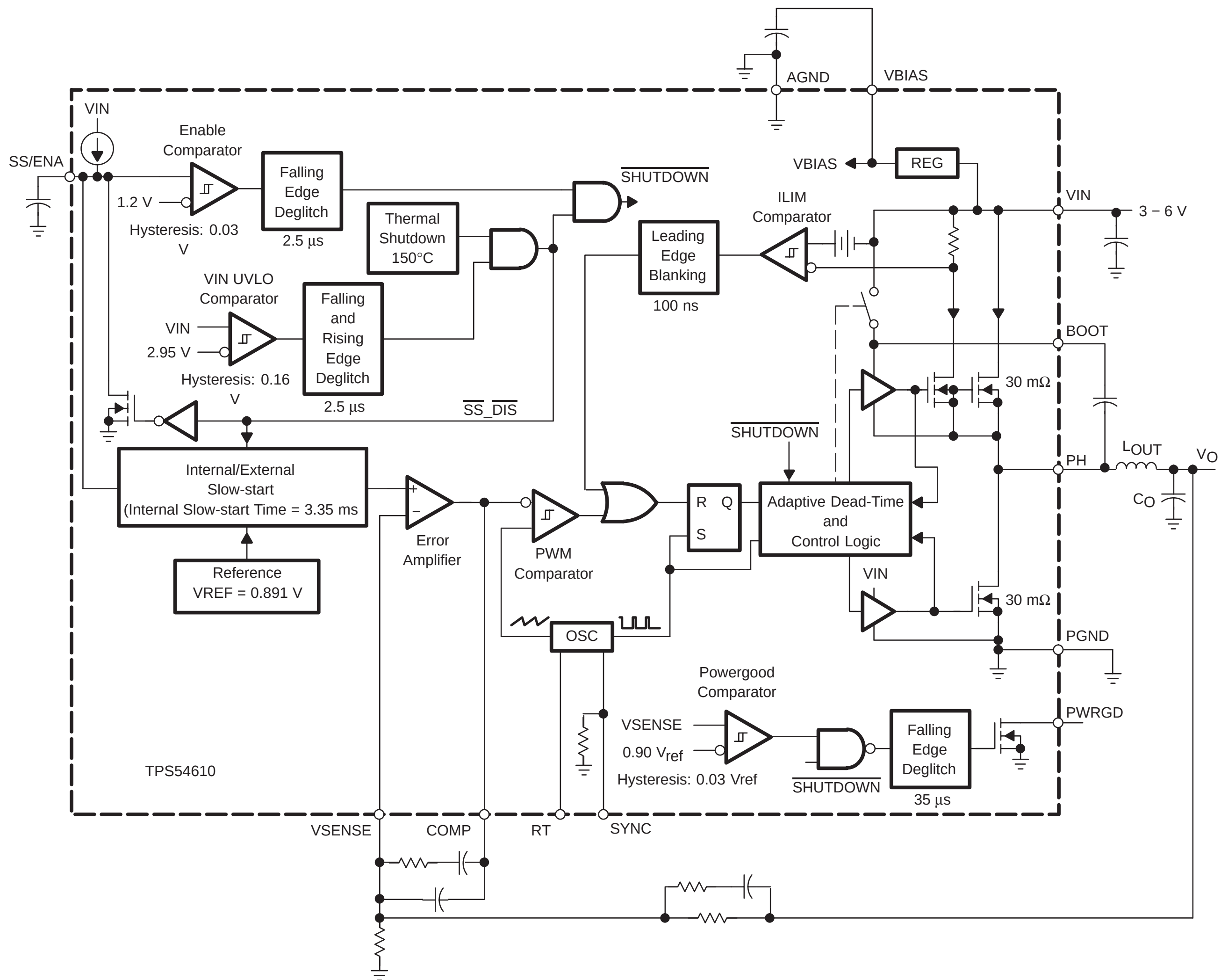
PWP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor and SYNC pin. Connect PowerPAD to AGND.
BOOT	5	Bootstrap output. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
PGND	15−19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6−14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PWRGD	4	Power good open drain output. High when VSENSE ≥ 90% V_{ref}, otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency. When using the SYNC pin, set the RT value for a frequency at or slightly lower than the external oscillator frequency.
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
SYNC	27	Synchronization input. Dual function pin which provides logic input to synchronize to an external oscillator or pin select between two internally set switching frequencies. When used to synchronize to an external signal, a resistor must be connected to the RT pin.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1-µF to 1.0-µF ceramic capacitor.
VIN	20−24	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low-ESR 10-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage through compensation network/output divider.

INTERNAL BLOCK DIAGRAM



ADDITIONAL 6A SWIFT™ DEVICES, (REFER TO SLVS397 AND SLVS400)

DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE	DEVICE	OUTPUT VOLTAGE
TPS54611	0.9 V	TPS54614	1.8 V	TPS54672	DDR memory/Adjustable
TPS54612	1.2 V	TPS54615	2.5 V	TPS54673	Prebias/adjustable
TPS54613	1.5 V	TPS54616	3.3 V	TPS54680	Sequencing/adjustable

RELATED DC/DC PRODUCTS

- TPS40000—Low-input, voltage-mode synchronous buck controller
- TPS759xx—7.5 A low dropout regulator
- PT6440 series—6 A plugin modules

TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

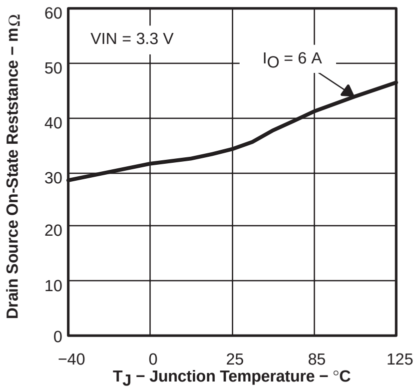


Figure 1

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

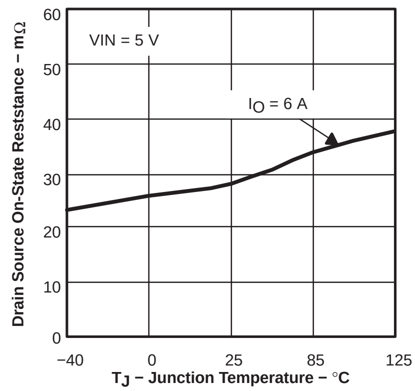


Figure 2

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

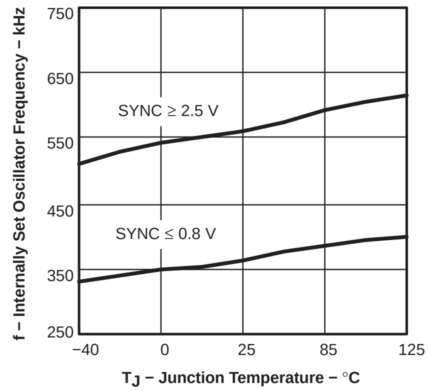


Figure 3

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

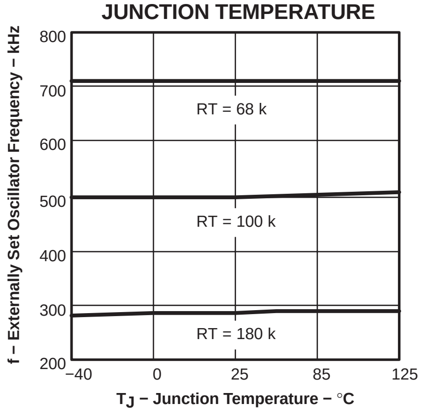


Figure 4

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

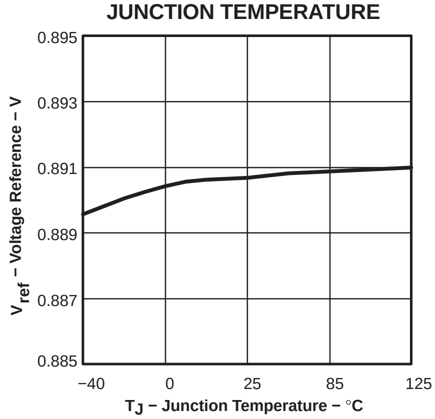


Figure 5

DEVICE POWER LOSSES AT T_J = 125°C vs LOAD CURRENT

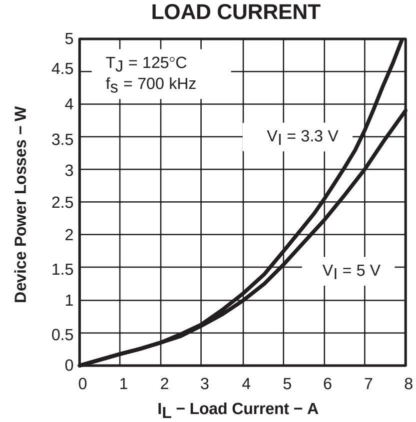


Figure 6

OUTPUT VOLTAGE REGULATION vs INPUT VOLTAGE

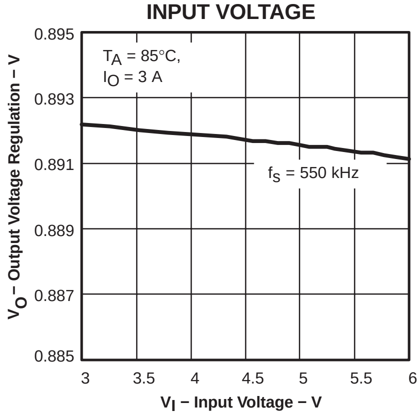


Figure 7

ERROR AMPLIFIER OPEN LOOP RESPONSE

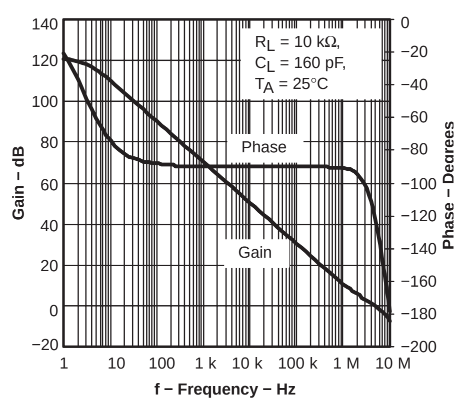


Figure 8

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

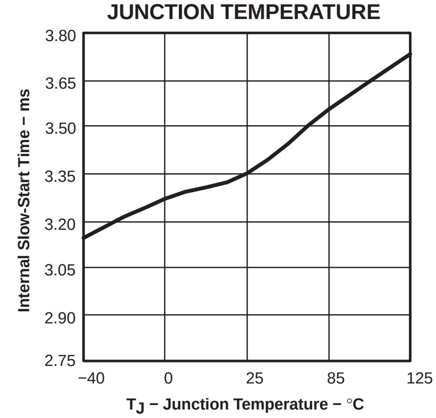


Figure 9

APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54610 application. The TPS54610 (U1) can provide greater than 6 A of output current at a nominal output voltage of 3.3 V. For proper thermal performance, the exposed thermal PowerPAD underneath the integrated circuit package must be soldered to the printed-circuit board.

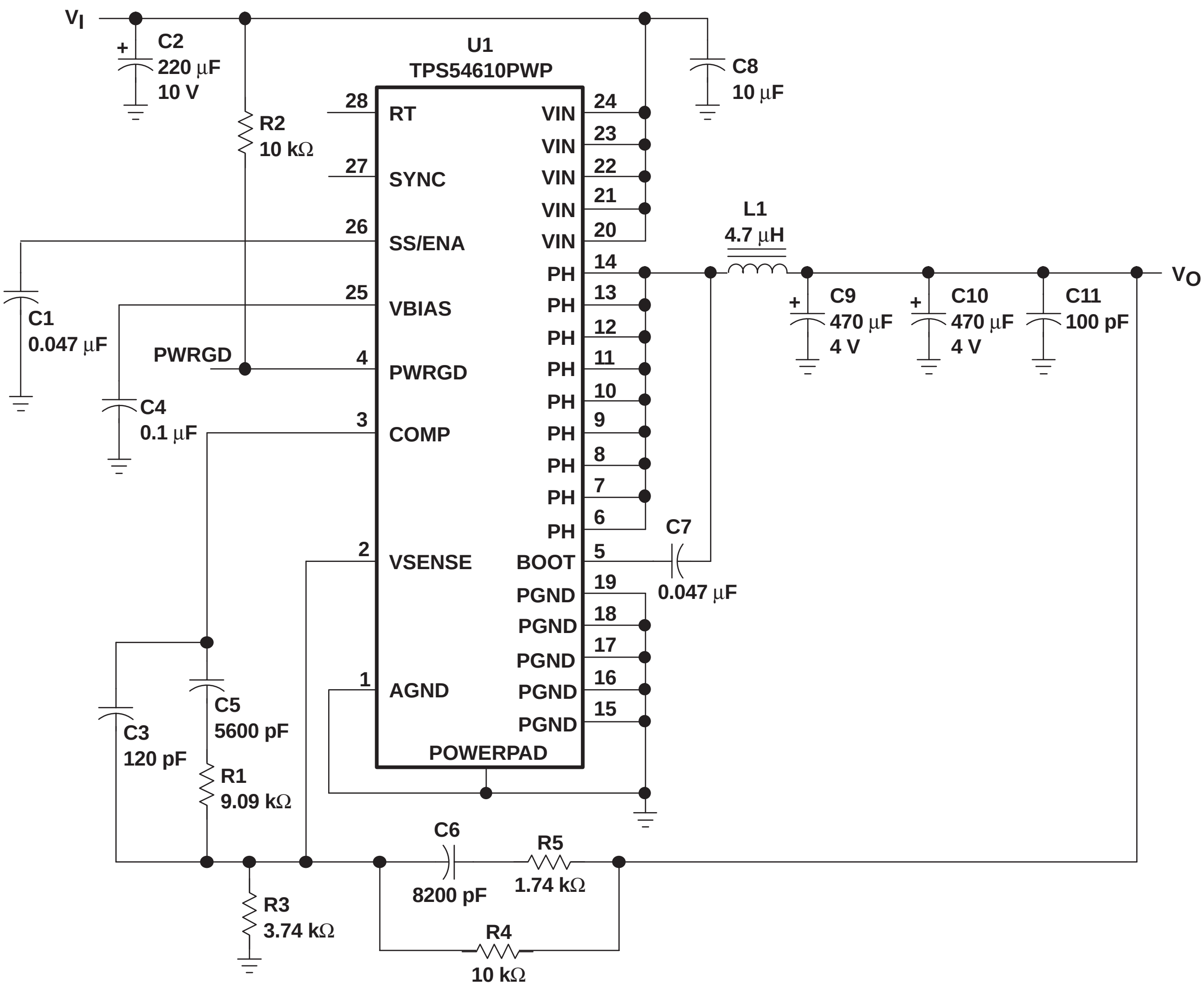


Figure 10. Application Circuit

COMPONENT SELECTION

The values for the components used in this design example were selected using the SWIFT designer software tool. SWIFT designer provides a complete design environment for developing dc-dc converters using the TPS54610.

INPUT FILTER

The input to the circuit is a nominal 5 VDC. The input filter C2 is a 220-µF POSCAP capacitor, with a maximum allowable ripple current of 3 A. C8 provides high frequency decoupling of the TPS54610 from the input supply and must be located as close as possible to the device. Ripple current is carried in both C2 and C8, and the return path to PGND must avoid the current circulating in the output capacitors C9 and C10.

FEEDBACK CIRCUIT

The resistor divider network of R3 and R4 sets the output voltage for the circuit at 3.3 V. R4, along with R1, R5, C3, C5, and C6 form the loop compensation network for the circuit. For this design, a Type 3 topology is used.

OPERATING FREQUENCY

In the application circuit, the 350 kHz operation is selected by leaving RT and SYNC open. Connecting a 180 kΩ to 68 kΩ resistor between RT (pin 28) and analog ground can be used to set the switching frequency to 280 kHz to 700 kHz. To calculate the RT resistor, use the equation below:

$$R = \frac{500\ \text{kHz}}{\text{Switching Frequency}} \times 100\ [\text{k}\Omega] \quad (1)$$

OUTPUT FILTER

The output filter is composed of a 4.7-µH inductor and two 470-µF capacitors. The inductor is a low dc resistance (12 mΩ) type, Coiltronics UP3B−4R7. The capacitors used are 4 V POSCAP types with a maximum ESR of 0.040 Ω. The feedback loop is compensated so that the unity gain frequency is approximately 25 kHz.

GROUNDING AND POWERPAD LAYOUT

The TPS54610 has two internal grounds (analog and power). Inside the TPS54610, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD must be tied directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54610, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. Therefore, separate analog and power ground planes are recommended. These two planes must tie together directly at the IC to reduce noise between the two grounds.

The only components that must tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54610. The layout of the TPS54610 evaluation module is representative of a recommended layout for a 4-layer board. Documentation for the TPS54610 evaluation module can be found on the Texas Instruments web site under the TPS54610 product folder. See the TPS54610 EVM user's guide, *TI literature number SLVU054*, and the application note, *TI literature number SLVA104*.

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide an adequate heat dissipating area. A 3-inch by 3-inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer must be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Eight vias must be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the twelve recommended that enhance thermal performance must be included in areas not under the device package.

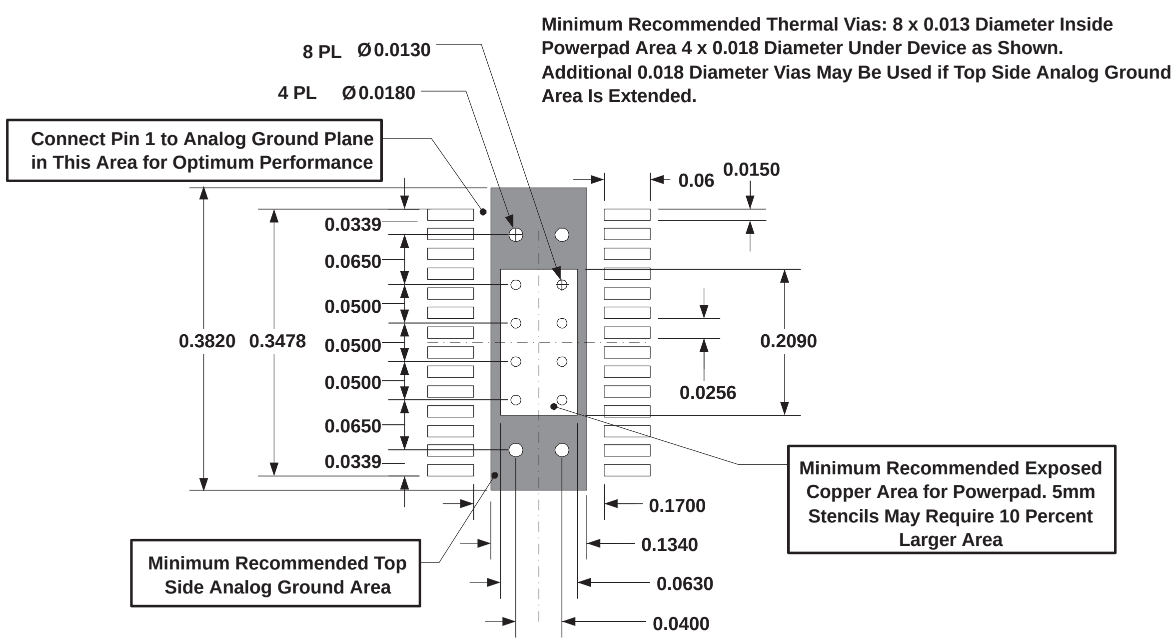


Figure 11. Recommended Land Pattern for 28-Pin PWP PowerPAD

PERFORMANCE GRAPHS

EFFICIENCY vs OUTPUT CURRENT

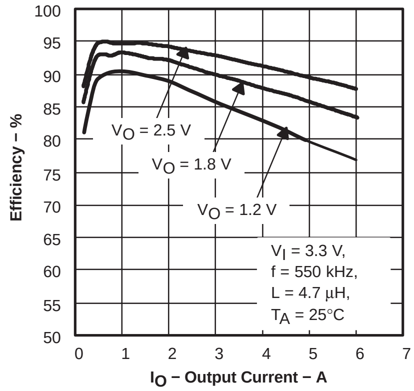


Figure 12

EFFICIENCY vs OUTPUT CURRENT

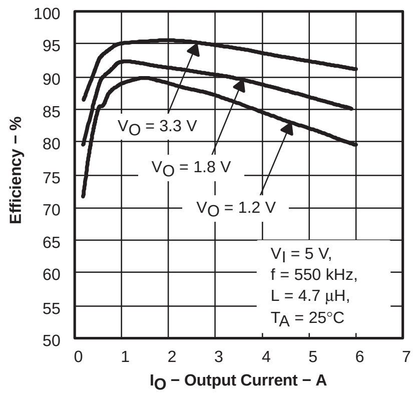


Figure 13

LOAD REGULATION vs OUTPUT CURRENT

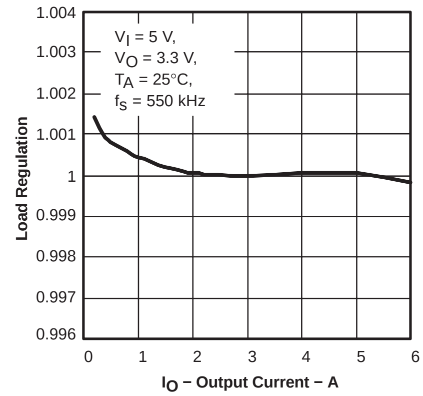


Figure 14

LINE REGULATION vs INPUT VOLTAGE

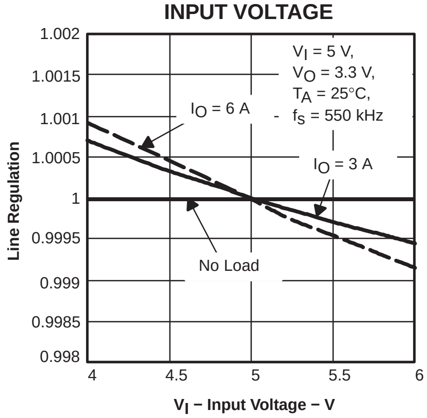


Figure 15

LOOP RESPONSE

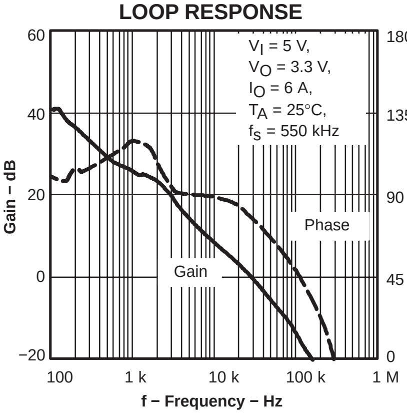


Figure 16

AMBIENT TEMPERATURE vs LOAD CURRENT

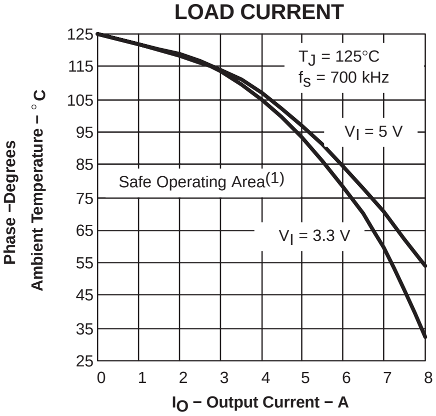


Figure 17

OUTPUT RIPPLE VOLTAGE

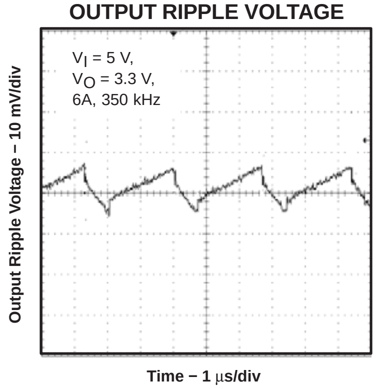


Figure 18

LOAD TRANSIENT RESPONSE

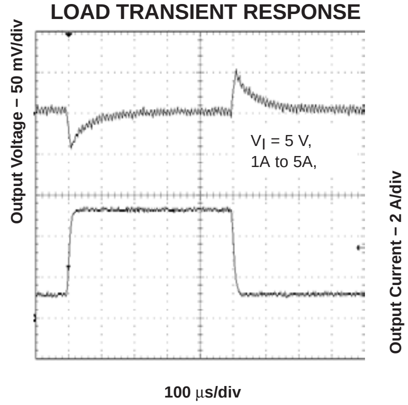


Figure 19

SLOW-START TIMING

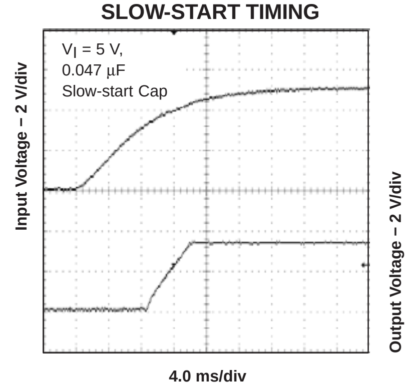


Figure 20

(1) Safe operating area is applicable to the test board conditions in the Dissipation Ratings

Figure 21 shows the schematic diagram for a reduced size, high frequency application using the TPS54610. The TPS54610 (U1) can provide up to 6 A of output current at a nominal output voltage of 1.8 V. A small size 0.56 uH inductor is used and the switching frequency is set to 680 kHz by R1. The compensation network is optimized for fast transient response as shown in Figure 21. For good thermal performance, the PowerPAD underneath the integrated circuit TPS54610 needs to be soldered well to the printed-circuit board. Application information is available in TI literature number SLVA107, *Designing for Small-Size, High-Frequency Applications With Swift*™ *Family of Synchronous Buck Regulators*.

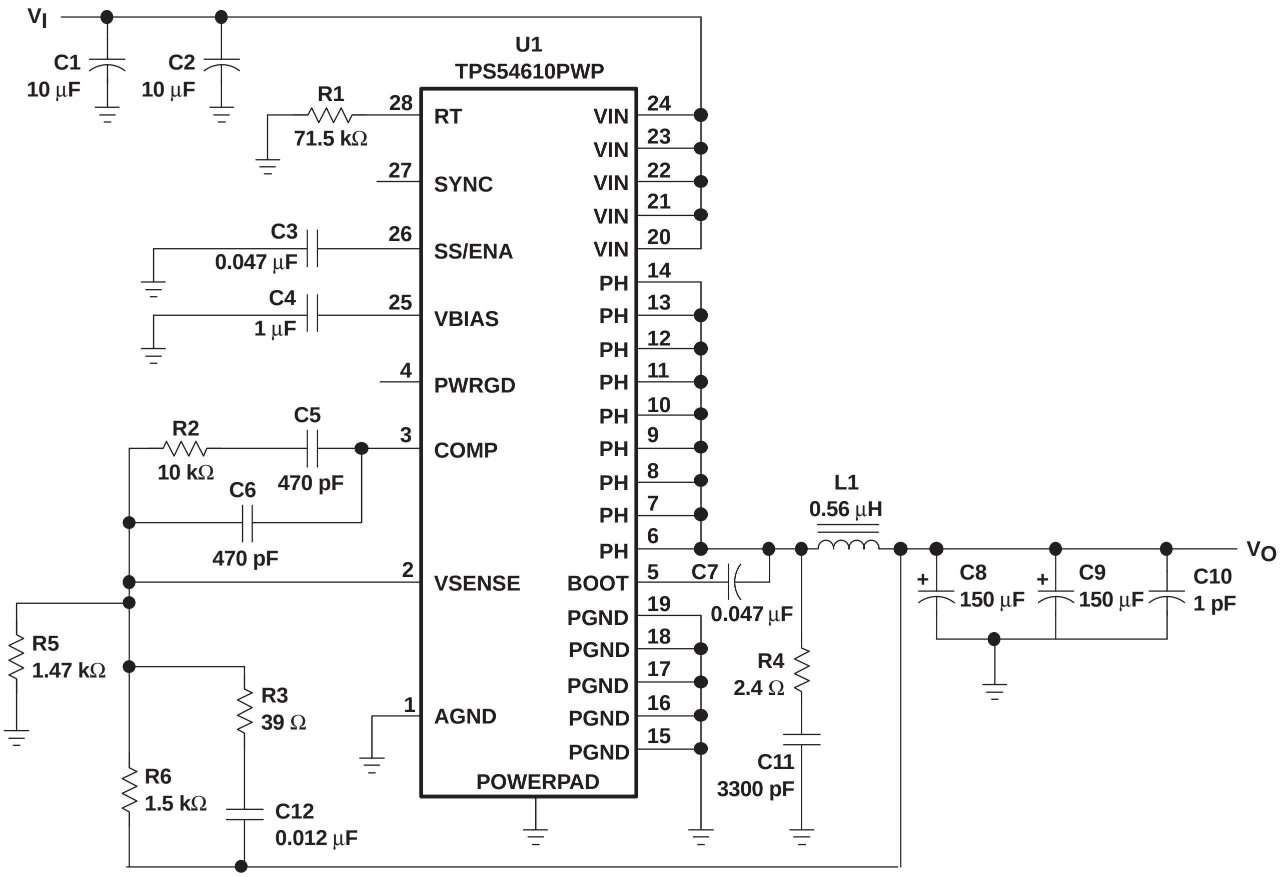


Figure 21. Small Size, High Frequency Design

TRANSIENT RESPONSE, 1.5-A to 4.5-A STEP

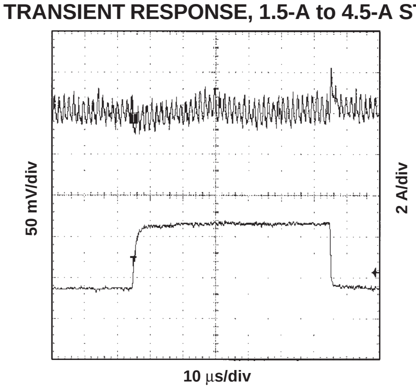


Figure 22

DETAILED DESCRIPTION

UNDERVOLTAGE LOCK OUT (UVLO)

The TPS54610 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

SLOW-START/ENABLE (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ \text{V}}{5\ \mu\text{A}} \qquad (2)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ \text{V}}{5\ \mu\text{A}} \qquad (3)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

VOLTAGE REFERENCE

The voltage reference system produces a precise V_{ref} signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54610, since it cancels offset errors in the scale and error amplifier circuits.

OSCILLATOR AND PWM RAMP

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the SYNC pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin and AGND and floating the SYNC pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{R} \times 500\ [\text{kHz}] \qquad (4)$$

External synchronization of the PWM ramp is possible over the frequency range of 330 kHz to 700 kHz by driving a synchronization signal into SYNC and connecting a resistor from RT to AGND. Choose a resistor between the RT and AGND which sets the free running frequency to 80% of the synchronization signal. The following table summarizes the frequency selection configurations:

SWITCHING FREQUENCY	SYNC PIN	RT PIN
350 kHz, internally set	Float or AGND	Float
550 kHz, internally set	≥ 2.5 V	Float
Externally set 280 kHz to 700 kHz	Float	R = 180 kΩ to 68 kΩ
Externally synchronized frequency	Synchronization signal	R = RT value for 80% of external synchronization frequency

ERROR AMPLIFIER

The high performance, wide bandwidth, voltage error amplifier sets the TPS54610 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is reset, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54610 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

THERMAL SHUTDOWN

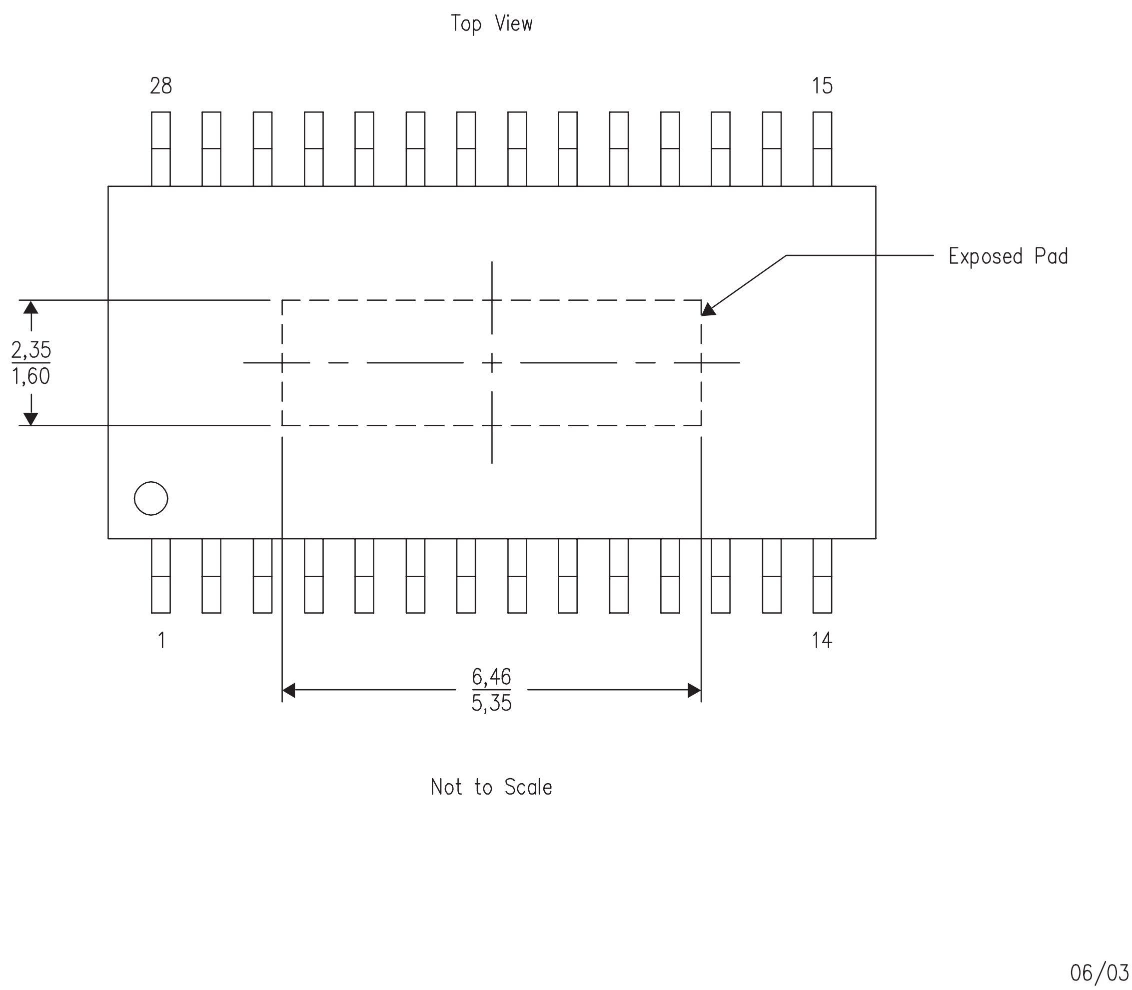
The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

POWER-GOOD (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low, or a thermal shutdown occurs. When VIN ≥ UVLO threshold, SS/ENA ≥ enable threshold, and VSENSE > 90% of V_{ref}, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35 µs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

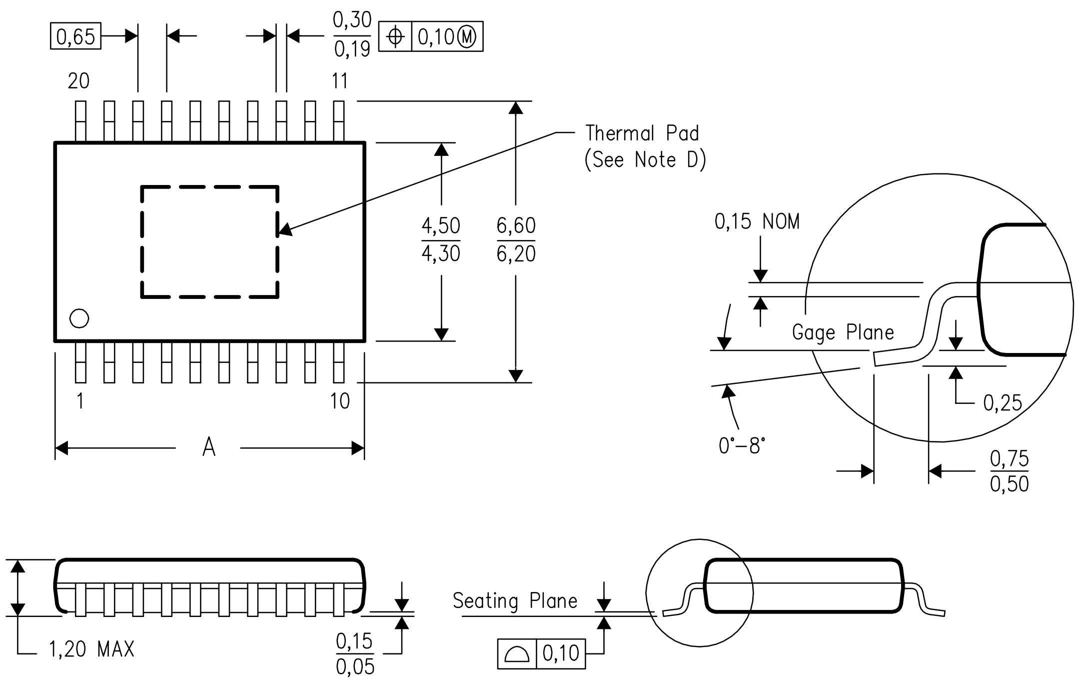
PWP (R−PDSO−G28) **PowerPAD™ PLASTIC SMALL−OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, ***PowerPAD Thermally Enhanced Package***, Texas Instruments Literature No. SLMA002 and Application Brief, ***PowerPAD Made Easy***, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO-153

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